AT91SAM9263-EK Evaluation Board

User Guide

6325D–ATARM–26-Aug-09

Table of Contents

Section 1

Overview

1.1 Scope

The AT91SAM9263-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9263.

This guide focuses on the AT91SAM9263-EK board as an evaluation platform.

1.2 Deliverables

The AT91SAM9263-EK package contains the following items:

- an AT91SAM9263-EK board
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM9263-EK Evaluation Board

The board is equipped with an AT91SAM9263 (324-ball LFBGA package) together with the following:

- 64 Mbytes of SDRAM memory
- 4 Mbytes of PSRAM memory on EBI1
- 256 Mbytes of NANDFlash memory
- One NOR Flash memory (footprint only)
- One 1.8” Hard disk connectors
- One TWI serial memory
- One USB device port interface
- Two USB Host port interfaces
- One RS232 serial communication port
- One DBGU serial communication port
- One serial CAN 2.0B communication port
- One JTAG/ICE debug interface
- One Ethernet 100-base TX with three status LEDs
- One AC97 Audio DAC

- One 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- One ISI connector (camera interface)
- One Power LED and two general-purpose LEDs
- Two user input push buttons
- One Wakeup input push button
- One reset push button
- One DataFlash®/SD/SDIO/MMC card slot
- One SD/SDIO/MMC card slot
- One Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9263-EK Board

2.1 Electrostatic Warning

The AT91SAM9263-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9263-EK evaluation board, the following items are needed:

- the AT91SAM9263-EK evaluation board itself.
- AC/DC power adapter (12V at 1A), 2.1 mm by 5.5 mm

2.3 Layout

See Figures 2-1 and 2-2.

Figure 2-1. AT91SAM9263-EK Layout - Top View

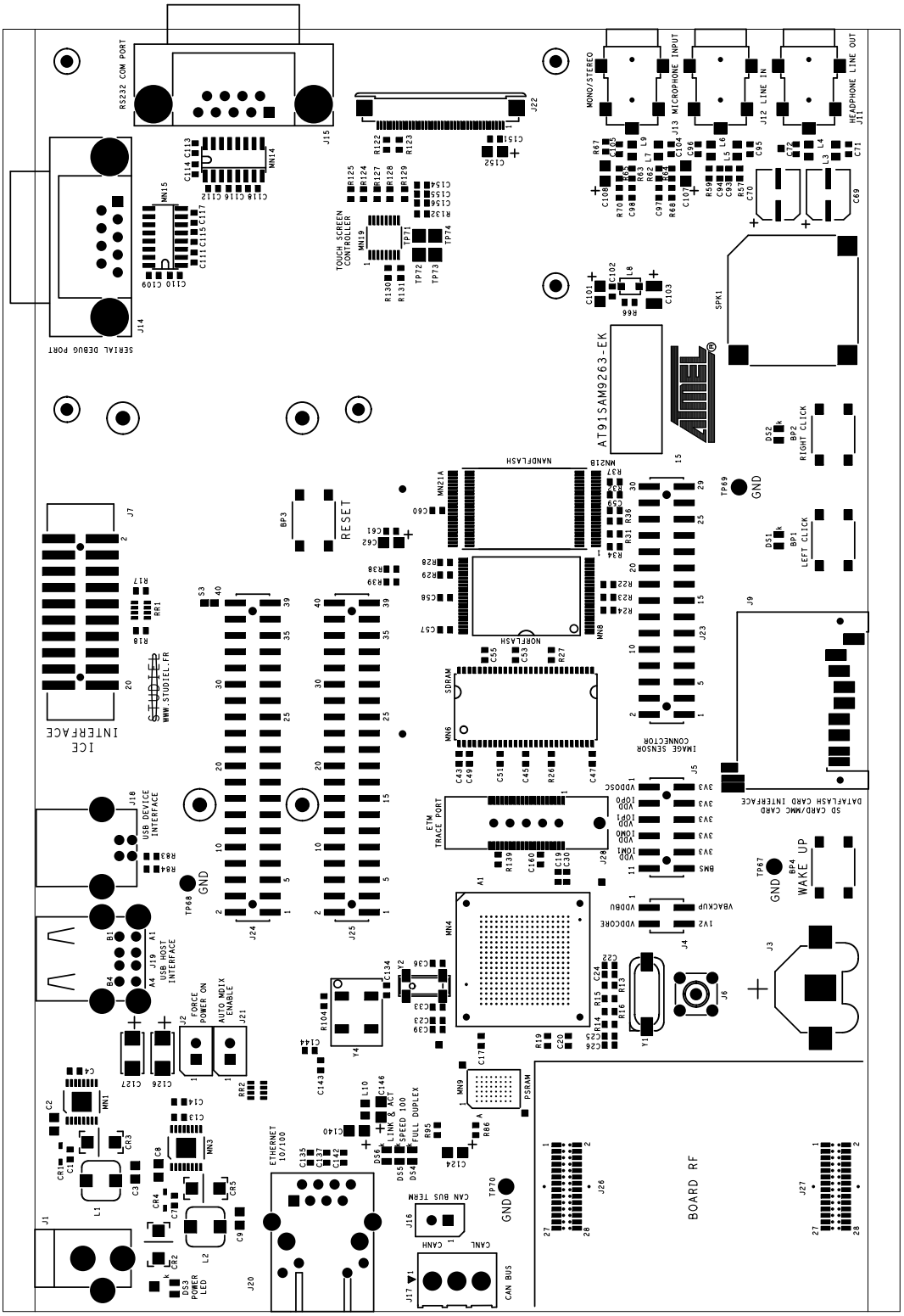
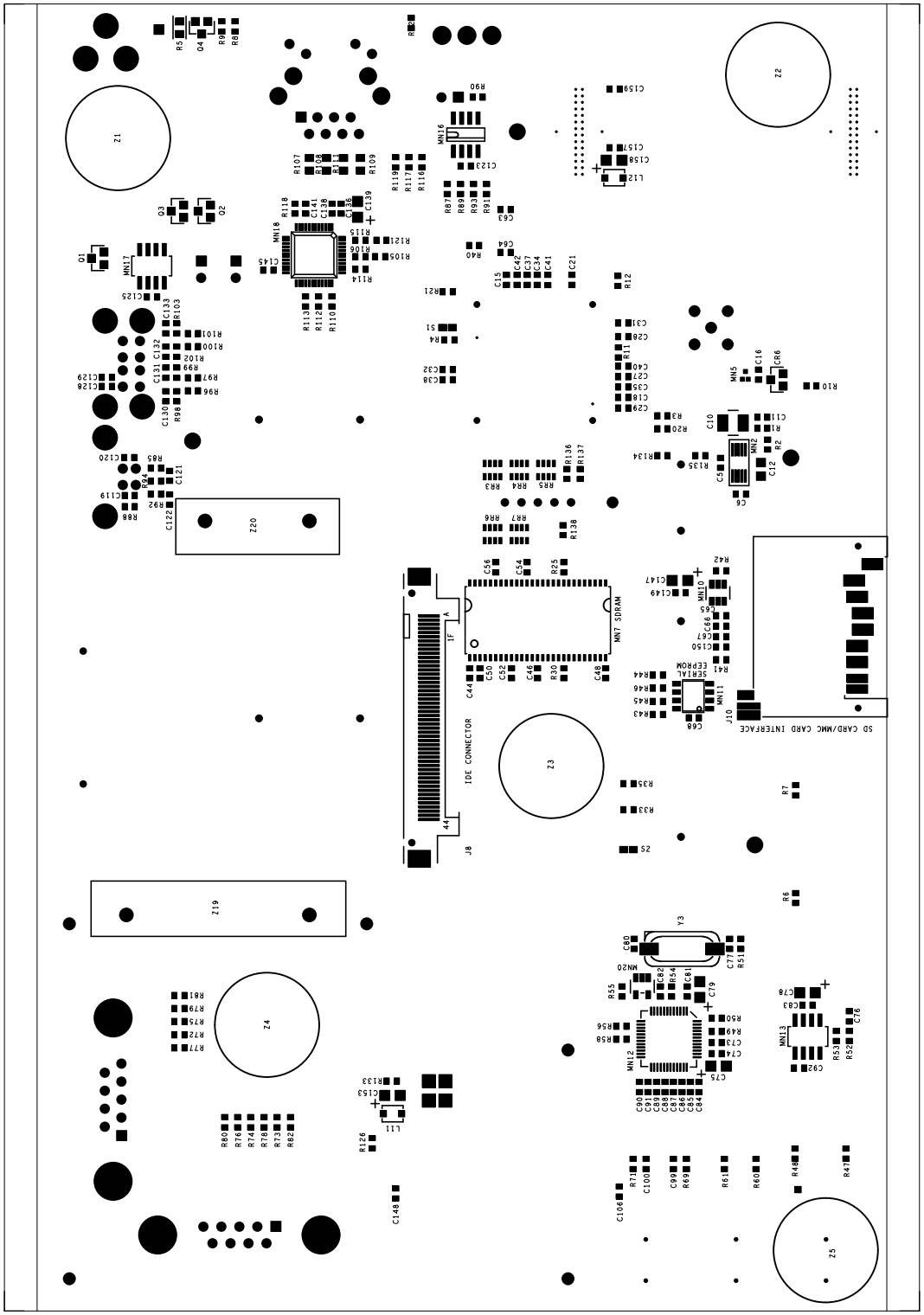


Figure 2-2. AT91SAM9263-EK Layout - Bottom View



2.4 Powering Up the Board

The AT91SAM9263-EK requires 12V DC. DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

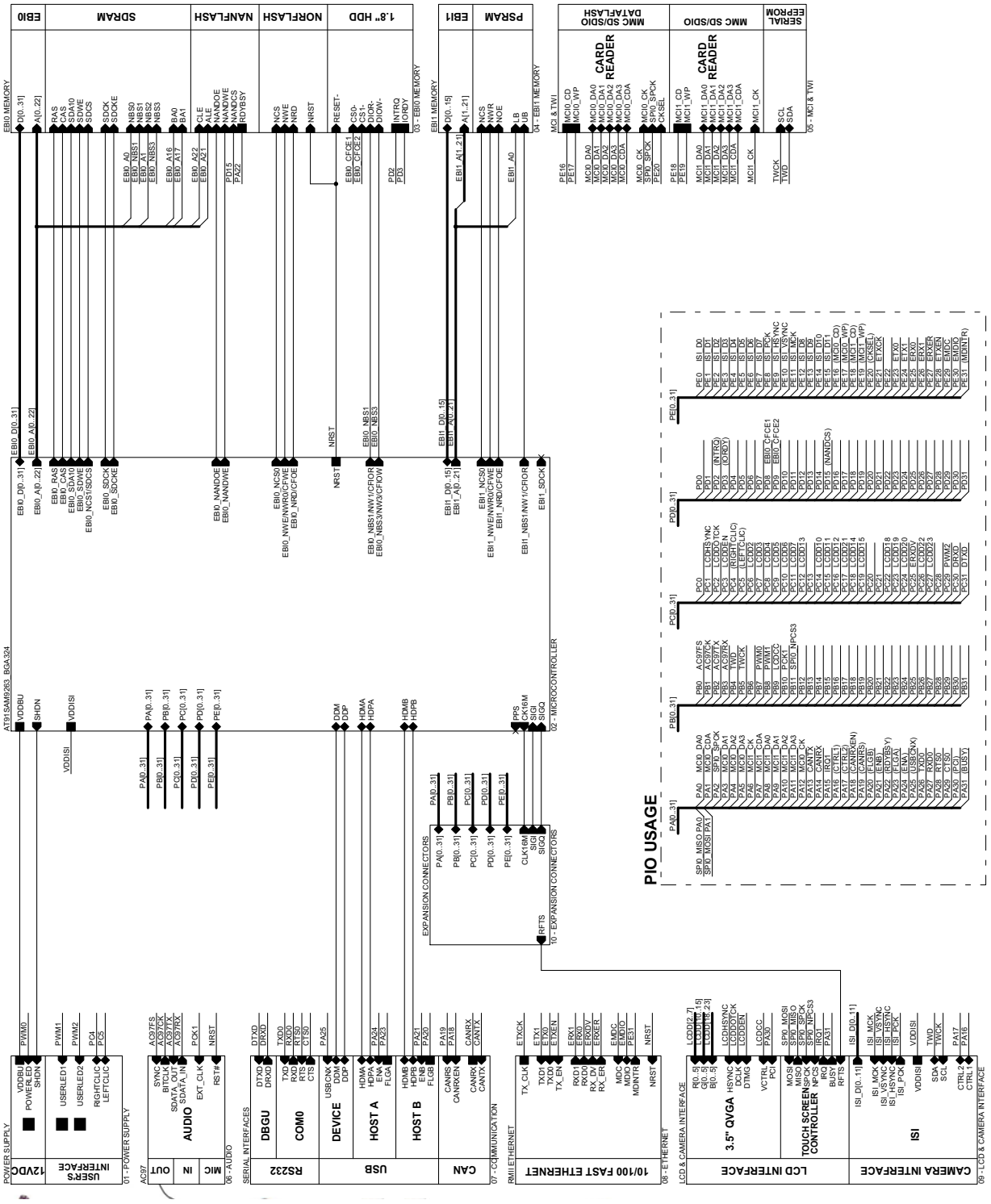
The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device.

2.6 Getting Started

The AT91SAM9263-EK evaluation board is delivered with a CD-ROM that allows the user to begin evaluation of the AT91 ARM Thumb 32-bit microcontroller quickly. Please refer to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM9263-EK.

2.7 AT91SAM9263-EK Block Diagram

Figure 2-3. AT91SAM9263-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9263 Microcontroller

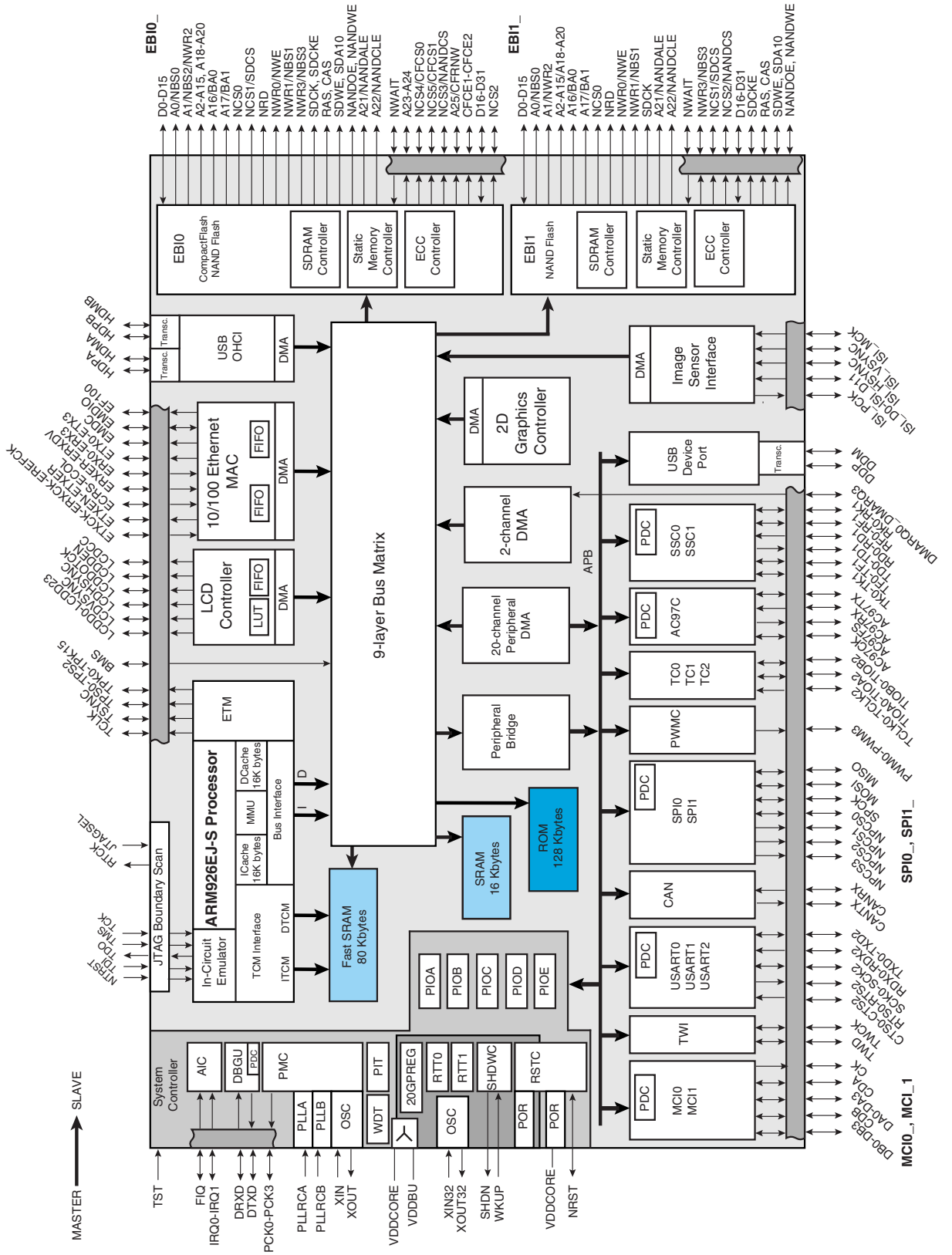
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, Jazelle® Technology for Java® Acceleration
  - 16 Kbyte Data Cache, 16 Kbyte Instruction Cache, Write Buffer
  - 200 MIPS at 180 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
  - Mid-level Implementation Embedded Trace Macrocell™
- Bus Matrix
  - Nine 32-bit-layer Matrix, Allowing a Total of 28.8 Gbps of On-chip Bus Bandwidth
  - Boot Mode Select Option, Remap Command
- Embedded Memories
  - One 128 Kbyte Internal ROM, Single-cycle Access at Maximum Bus Matrix Speed
  - One 80 Kbyte Internal SRAM, Single-cycle Access at Maximum Processor Bus Matrix Speed
  - One 16 Kbyte Internal SRAM, Single-cycle Access at Maximum Bus Matrix Speed
- Dual External Bus Interface (EBI0 and EBI1)
  - EBI0 Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
  - EBI1 Supports SDRAM, Static Memory and ECC-enabled NAND Flash
- DMA Controller (DMAC)
  - Acts as one Bus Matrix Master
  - Embeds 2 Unidirectional Channels with Programmable Priority, Address Generation, Channel Buffering and Control
- Twenty Peripheral DMA Controller Channels (PDC)
- LCD Controller
  - Supports Passive or Active Displays
  - Up to 24 bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Supports Virtual Screen Buffers
- 2D Graphics Accelerator
  - Line Draw, Block Transfer, Polygon Fill, Clipping, Commands Queuing
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format

- USB 2.0 Full Speed (12 Mbits per second) Host Double Port
  - Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Ethernet MAC 10/100 Base-T
  - Media Independent Interface or Reduced Media Independent Interface
  - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Double Real-time Timer
- Reset Controller (RSTC)
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and Two Up to 240 MHz PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Two Real-time Timers (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- Five 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC, PIOD and PIOE)
  - 160 Programmable I/O Lines Multiplexed with Up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- One Part 2.0A and Part 2.0B-compliant CAN Controller

  - 16 Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- Two Multimedia Card Interfaces (MCI)
  - SDCard/SDIO and MultiMediaCard Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
  - Two SDCard Slots Support on each Controller
- Two Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- One AC97 Controller (AC97C)
  - 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications at Up to 90Mbits/sec
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel® EEPROMs Supported
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 3.0V to 3.6V for VDDOSC, VDDPLL and VDDIOP0 (Peripheral I/Os)
  - 1.65V to 3.6V for VDDIOP1 (Peripheral I/Os)
  - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM0/VDDIOM1 (Memory I/Os)
- Available in a 324-ball BGA Green Package

3.2 AT91SAM9263 Block Diagram

Figure 3-1. AT91SAM9263 Block Diagram



3.3 Memory

- 16 Kbytes of Internal data cache
- 16 Kbytes of Internal instruction cache
- 128 Kbytes of Internal ROM
- 80 Kbytes of Internal single-cycle access high-speed SRAM
- 16 Kbytes of Internal single-cycle access high-speed SRAM
- 8 Mbytes of Atmel NOR Flash (not populated)
- 64 Mbytes of SDRAM memory
- 4 Mbytes of PSRAM (EBI1)
- 256 Mbytes of NANDFlash memory
- Atmel TWI serial EEPROM

3.4 Clock Circuitry

- 16.36766 MHz standard crystal for the embedded oscillator
- 32.768 kHz standard crystal for the slow clock oscillator

3.5 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.6 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM9263 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm.
- On-board 1.2V high efficiency step-down Charge Pump regulator with shutdown control
- On-board 3.3V switching regulator with shutdown control
- On-board 5V switching regulator with shutdown control

3.8 Remote Communication

- One RS232 serial communication port
- One serial CAN 2.0B communication port via 3-position printed circuit terminal block
- One USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
- Two USB Host ports V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
- One RMII Ethernet 100-base TX with three status LEDs

3.9 Audio Stereo Interface

- One AC'97 2.3 compliant Codec (20-bit PCM DAC)
- One 32-ohm Stereo Headset line-out
- One stereo line input
- One stereo electret microphone input
- One mono 8-ohm amplified speaker

3.10 User Interface

- Two user input pushbuttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)
- One 3.5" ¼ VGA display LCD with Touch Panel and white LED backlight
- One ISI connector (camera interface)

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket

3.12 Expansion Slot

- One DataFlash/SD/SDIO/MMC card slot
- One SD/SDIO/MMC card slot
- All unused I/Os of the AT91SAM9263 are routed to peripheral extension connectors (J24 and J25). This allows the developer to add external hardware components or boards.

3.13 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PA0	MCI0_DA0	SPI0_MISO	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH screen CONTROLLER	MCI0_DA0 or SPI0_MISO	VDDIOP0
PA1	MCI0_CDA	SPI0_MOSI	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH screen CONTROLLER	MCI0_CDA or SPI0_MOSI	VDDIOP0
PA2		SPI0_SPCK	SD/MMC/DATAFLASH SOCKET (J9) & TOUCH screen CONTROLLER	SPI0_SPCK	VDDIOP0
PA3	MCI0_DA1	SPI0_NPCS1	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA4	MCI0_DA2	SPI0_NPCS2	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA5	MCI0_DA3	SPI0_NPCS0	SD/MMC/DATAFLASH SOCKET (J9)		VDDIOP0
PA6	MCI1_CK	PCK2	SD/MMC SOCKET (J10)	MCI1_CK	VDDIOP0
PA7	MCI1_CDA		SD/MMC SOCKET (J10)	MCI1_CDA	VDDIOP0
PA8	MCI1_DA0		SD/MMC SOCKET (J10)	MCI1_DA0	VDDIOP0
PA9	MCI1_DA1		SD/MMC SOCKET (J10)	MCI1_DA1	VDDIOP0
PA10	MCI1_DA2		SD/MMC SOCKET (J10)	MCI1_DA2	VDDIOP0
PA11	MCI1_DA3		SD/MMC SOCKET (J10)	MCI1_DA3	VDDIOP0
PA12	MCI0_CK		SD/MMC/DATAFLASH SOCKET (J9)	MCI0_CK	VDDIOP0
PA13	CANTX	PCK0	CAN BUS INTERFACE (J17)	CANTX	VDDIOP0
PA14	CANRX	IRQ0	CAN BUS INTERFACE (J17)	CANRX	VDDIOP0
PA15	TCLK2	IRQ1	TOUCH SCREEN CONTROLLER (MN19)	IRQ1	VDDIOP0
PA16	MCI0_CDB	EBI1_D16	IMAGE SENSORS CONNECTORS (J23)	PA16 as CTRL1	VDDIOM1
PA17	MCI0_DB0	EBI1_D17	IMAGE SENSORS CONNECTORS (J23)	PA17 as CTRL2	VDDIOM1
PA18	MCI0_DB1	EBI1_D18	CAN INTERFACE (RXEN)	PA18 as RXEN	VDDIOM1
PA19	MCI0_DB2	EBI1_D19	CAN INTERFACE (RS)	PA19 as RS	VDDIOM1
PA20	MCI0_DB3	EBI1_D20	USB HOST B POWER MONITOR (MN17)	PA20 as FLGB	VDDIOM1
PA21	MCI1_CDB	EBI1_D21	USB HOST B POWER CONTROL (MN17)	PA21 as ENB	VDDIOM1
PA22	MCI1_DB0	EBI1_D22	NANDFLASH (MN12B)	PA22 as RDY/BSY	VDDIOM1
PA23	MCI1_DB1	EBI1_D23	USB HOST B POWER MONITOR (MN17)	PA23 as FLGA	VDDIOM1
PA24	MCI1_DB2	EBI1_D24	USB HOST B POWER CONTROL (MN17)	PA24 as ENA	VDDIOM1
PA25	MCI1_DB3	EBI1_D25	USB DEVICE INTERFACE	PA25 as USB_CNX	VDDIOM1
PA26	TXD0	EBI1_D26	RS232 COM PORT (J15)	TXD0	VDDIOM1
PA27	RXD0	EBI1_D27	RS232 COM PORT (J15)	RXD0	VDDIOM1
PA28	RTS0	EBI1_D28	RS232 COM PORT (J15)	RTS0	VDDIOM1
PA29	CTS0	EBI1_D29	RS232 COM PORT (J15)	CTS0	VDDIOM1
PA30	SCK0	EBI1_D30	LCD PANEL (Power Control In)	PA30 as PCI	VDDIOM1
PA31	DMARQ0	EBI_D31	TOUCH SCREEN CONTROLLER (MN19)	PA31 as BUSY	VDDIOM1

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PB0	AC97FS	TF0	AC97 CODEC (MN12)	AC97FS	VDDIOP0
PB1	AC97CK	TK0	AC97 CODEC (MN12)	AC97CK	VDDIOP0
PB2	AC97TX	TD0	AC97 CODEC (MN12)	AC97TX	VDDIOP0
PB3	AC97RX	RD0	AC97 CODEC (MN12)	AC97RX	VDDIOP0
PB4	TWD	RK0	TWI EEPROM (MN11)	TWD / SDA	VDDIOP0
PB5	TWCK	RF0	TWI EEPROM (MN11)	TWCK / SCL	VDDIOP0
PB6	TF1	DMARQ1			VDDIOP0
PB7	TK1	PWM0	POWER LED CONTROL (DS3)	PB7 or PWM0	VDDIOP0
PB8	TD1	PWM1	USER'S LED1 CONTROL (DS1)	PB8 or PWM1	VDDIOP0
PB9	RD1	LCDCC	LCD PANEL (backlight control)	LCDCC	VDDIOP0
PB10	RK1	PCK1	AC97 CODEC (MN12) Optional clock source	PCK1	VDDIOP0
PB11	RF1	SPI0_NPCS3	TOUCH SCREEN CONTROLLER (MN19)	SPI0_NPCS3	VDDIOP0
PB12	SPI1_MISO				VDDIOP0
PB13	SPI1_MOSI				VDDIOP0
PB14	SPI1_SPCK				VDDIOP0
PB15	SPI1_NPCS0				VDDIOP0
PB16	SPI1_NPCS1	PCK1			VDDIOP0
PB17	SPI1_NPCS2	TIOA2			VDDIOP0
PB18	SPI1_NPCS3	TIOB2			VDDIOP0
PB19					VDDIOP0
PB20					VDDIOP0
PB21					VDDIOP0
PB22					VDDIOP0
PB23					VDDIOP0
PB24		DMARQ3			VDDIOP0
PB25					VDDIOP0
PB26					VDDIOP0
PB27		PWM2			VDDIOP0
PB28		TCLK0			VDDIOP0
PB29		PWM3			VDDIOP0
PB30					VDDIOP0
PB31					VDDIOP0

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Peripheral Usage			Powered by
PC0	LCDVSYNC					VDDIOP0
PC1	LCDHSYNC		LCD PANEL	LCDHSYNC		VDDIOP0
PC2	LCDDOTCK		LCD PANEL	LCDDOTCK		VDDIOP0
PC3	LCDDEN	PWM1	LCD PANEL	LCDDEN		VDDIOP0
PC4	LCDD0	LCDD3	USER'S PUSH BUTTON (BP2)	PC4 as RIGHT CLICK		VDDIOP0
PC5	LCDD1	LCDD4	USER'S PUSH BUTTON (BP1)	PC5 as LEFT CLICK		VDDIOP0
PC6	LCDD2	LCDD5	LCD PANEL	LCDD2	RED	VDDIOP0
PC7	LCDD3	LCDD6	LCD PANEL	LCDD3	RED	VDDIOP0
PC8	LCDD4	LCDD7	LCD PANEL	LCDD4	RED	VDDIOP0
PC9	LCDD5	LCDD10	LCD PANEL	LCDD5	RED	VDDIOP0
PC10	LCDD6	LCDD11	LCD PANEL	LCDD6	RED	VDDIOP0
PC11	LCDD7	LCDD12	LCD PANEL	LCDD7	RED	VDDIOP0
PC12	LCDD8	LCDD13	LCD PANEL	LCDD13	GREEN	VDDIOP0
PC13	LCDD9	LCDD14				VDDIOP0
PC14	LCDD10	LCDD15	LCD PANEL	LCDD10	GREEN	VDDIOP0
PC15	LCDD11	LCDD19	LCD PANEL	LCDD11	GREEN	VDDIOP0
PC16	LCDD12	LCDD20	LCD PANEL	LCDD12	GREEN	VDDIOP0
PC17	LCDD13	LCDD21	LCD PANEL	LCDD21	BLUE	VDDIOP0
PC18	LCDD14	LCDD22	LCD PANEL	LCDD14	GREEN	VDDIOP0
PC19	LCDD15	LCDD23	LCD PANEL	LCDD15	GREEN	VDDIOP0
PC20	LCDD16	ETX2				VDDIOP0
PC21	LCDD17	ETX3				VDDIOP0
PC22	LCDD18	ERX2	LCD PANEL	LCDD18	BLUE	VDDIOP0
PC23	LCDD19	ERX3	LCD PANEL	LCDD19	BLUE	VDDIOP0
PC24	LCDD20	ETXER	LCD PANEL	LCDD20	BLUE	VDDIOP0
PC25	LCDD21	ERXDV	ETHERNET RMII (MN18)	ERXDV		VDDIOP0
PC26	LCDD22	ECOL	LCD PANEL	LCDD22	BLUE	VDDIOP0
PC27	LCDD23	ERXCK	LCD PANEL	LCDD23	BLUE	VDDIOP0
PC28	PWM0	TCLK1				VDDIOP0
PC29	PCK0	PWM2	USER'S LED2 CONTROL (DS2)	PC29 or PWM2		VDDIOP0
PC30	DRXD		SERIAL DEBUG PORT (J14)	DRXD		VDDIOP0
PC31	DTXD		SERIAL DEBUG PORT (J14)	DTXD		VDDIOP0

Table 3-4. PIO Controller D

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PD0	TXD1	SPI0_NPCS2			VDDIOP0
PD1	RXD1	SPI0_NPCS3			VDDIOP0
PD2	TXD2	SPI1_NPCS2	HDD CONNECTORS (J8)	PD2 as IRQ	VDDIOP0
PD3	RXD2	SPI1_NPCS3	HDD CONNECTORS (J8)	PD3 as IOREADY	VDDIOP0
PD4	FIQ	DMARQ2			VDDIOP0
PD5	EBI0_NWAIT	RTS2			VDDIOM0
PD6	EBI0_NCS4/CFCS0	CTS2			VDDIOM0
PD7	EBI0_NCS5/CFCS1	RTS1			VDDIOM0
PD8	EBI0_CFCE1	CTS1	HDD CONNECTORS (J8)	EBI0_CFCE1	VDDIOM0
PD9	EBI0_CFCE2	SCK2	HDD CONNECTORS (J8)	EBI0_CFCE2	VDDIOM0
PD10		SCK1			VDDIOM0
PD11	EBI0_NCS2	TSYNC			VDDIOM0
PD12	EBI0_A23	TCLK			VDDIOM0
PD13	EBI0_A24	TPS0			VDDIOM0
PD14	EBI0_A25_CFRNW	TPS1			VDDIOM0
PD15	EBI0_NCS3/NANDCS	TPS2	NANDFLASH (MN12B)	EBI0_NCS3/NANDCS	VDDIOM0
PD16	EBI0_D16	TPK0	EBI0 SDRAM DATA BUS	D16	VDDIOM0
PD17	EBI0_D17	TPK1	EBI0 SDRAM DATA BUS	D17	VDDIOM0
PD18	EBI0_D18	TPK2	EBI0 SDRAM DATA BUS	D18	VDDIOM0
PD19	EBI0_D19	TPK3	EBI0 SDRAM DATA BUS	D19	VDDIOM0
PD20	EBI0_D20	TPK4	EBI0 SDRAM DATA BUS	D20	VDDIOM0
PD21	EBI0_D21	TPK5	EBI0 SDRAM DATA BUS	D21	VDDIOM0
PD22	EBI0_D22	TPK6	EBI0 SDRAM DATA BUS	D22	VDDIOM0
PD23	EBI0_D23	TPK7	EBI0 SDRAM DATA BUS	D23	VDDIOM0
PD24	EBI0_D24	TPK8	EBI0 SDRAM DATA BUS	D24	VDDIOM0
PD25	EBI0_D25	TPK9	EBI0 SDRAM DATA BUS	D25	VDDIOM0
PD26	EBI0_D26	TPK10	EBI0 SDRAM DATA BUS	D26	VDDIOM0
PD27	EBI0_D27	TPK11	EBI0 SDRAM DATA BUS	D27	VDDIOM0
PD28	EBI0_D28	TPK12	EBI0 SDRAM DATA BUS	D28	VDDIOM0
PD29	EBI0_D29	TPK13	EBI0 SDRAM DATA BUS	D29	VDDIOM0
PD30	EBI0_D30	TPK14	EBI0 SDRAM DATA BUS	D30	VDDIOM0
PD31	EBI0_D31	TPK15	EBI0 SDRAM DATA BUS	D31	VDDIOM0

Table 3-5. PIO Controller E

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PE0	ISI_D0		IMAGE SENSORS CONNECTORS (J23)	ISI_D0	VDDIOP1
PE1	ISI_D1		IMAGE SENSORS CONNECTORS (J23)	ISI_D1	VDDIOP1
PE2	ISI_D2		IMAGE SENSORS CONNECTORS (J23)	ISI_D2	VDDIOP1
PE3	ISI_D3		IMAGE SENSORS CONNECTORS (J23)	ISI_D3	VDDIOP1
PE4	ISI_D4		IMAGE SENSORS CONNECTORS (J23)	ISI_D4	VDDIOP1
PE5	ISI_D5		IMAGE SENSORS CONNECTORS (J23)	ISI_D5	VDDIOP1
PE6	ISI_D6		IMAGE SENSORS CONNECTORS (J23)	ISI_D6	VDDIOP1
PE7	ISI_D7		IMAGE SENSORS CONNECTORS (J23)	ISI_D7	VDDIOP1
PE8	ISI_PCK	TIOA1	IMAGE SENSORS CONNECTORS (J23)	ISI_PCK	VDDIOP1
PE9	ISI_HSYNC	TIOB1	IMAGE SENSORS CONNECTORS (J23)	ISI_HSYNC	VDDIOP1
PE10	ISI_VSYNC	PWM3	IMAGE SENSORS CONNECTORS (J23)	ISI_VSYNC	VDDIOP1
PE11	ISI_MCK	PCK3	IMAGE SENSORS CONNECTORS (J23)	ISI_MCK	VDDIOP1
PE12		ISI_D8	IMAGE SENSORS CONNECTORS (J23)	ISI_D8	VDDIOP1
PE13		ISI_D9	IMAGE SENSORS CONNECTORS (J23)	ISI_D9	VDDIOP1
PE14		ISI_D10	IMAGE SENSORS CONNECTORS (J23)	ISI_D10	VDDIOP1
PE15		ISI_D11	IMAGE SENSORS CONNECTORS (J23)	ISI_D11	VDDIOP1
PE16			SD/MMC/DATAFLASH SOCKET (J9)	PE16 as CD (Card Detect)	VDDIOP1
PE17			SD/MMC/DATAFLASH SOCKET (J9)	PE17 as WP (Write Protect)	VDDIOP1
PE18		TIOA0	SD/MMC SOCKET (J10)	PE18 as CD (Card Detect)	VDDIOP1
PE19		TIOB0	SD/MMC SOCKET (J10)	PE19 as WP (Write Protect)	VDDIOP1
PE20		EBI1_NWAIT	SD/MMC/DATAFLASH SOCKET (J9)	PE20 as CKSEL (Clock Select)	VDDIOM1
PE21	ETXCK	EBI1_NANDWE	ETHERNET RMII (MN18)	ETXCK	VDDIOM1
PE22	ECRS	EBI1_NCS2/NANDCS			VDDIOM1
PE23	ETX0	EB1_NANDOE	ETHERNET RMII (MN18)	ETX0	VDDIOM1
PE24	ETX1	EBI1_NWR3/NBS3	ETHERNET RMII (MN18)	ETX1	VDDIOM1
PE25	ERX0	EBI1_NCS1/SDCS	ETHERNET RMII (MN18)	ERX0	VDDIOM1
PE26	ERX1			ERX1	VDDIOM1
PE27	ERXER	EBI1_SDCKE	ETHERNET RMII (MN18)	ERXER	VDDIOM1
PE28	ETXEN	EBI1_RAS	ETHERNET RMII (MN18)	ETXEN	VDDIOM1
PE29	EMDC	EBI1_CAS	ETHERNET RMII (MN18)	EMDC	VDDIOM1
PE30	EMDIO	EBI1_SDWE	ETHERNET RMII (MN18)	EMDIO	VDDIOM1
PE31	EF100	EBI1_SDA10	ETHERNET RMII (MN18)	PE31 as IRQ	VDDIOM1

Section 4

Configuration

4.1 Configuration Jumpers and Straps

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	Forces power on. To use the software shutdown control, J2 must be opened and the battery backup inserted in its socket.
J4-1	Closed	VDDBU jumper (1)
J4-2	Closed	VDDCORE jumper (1)
J5-1	Closed	VDDOSC jumper (1)
J5-2	Closed	VDDIOP0 jumper(1)
J5-3	Closed	VDDIOP1 jumper(1)
J5-4	Closed	VDDIOM0 jumper (1)
J5.5	Closed	VDDIOM1 jumper (1)
J5-6	Opened	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J16	Closed	Enables 120 ohms CAN bus resistance termination
J21	Closed	Enables Ethernet Auto MDIX control
S1	Opened	Selects ICE mode. See Section 7, “Errata”
S2	Opened	Disables NAND FLASH write protect
S3	Opened	Disables 5V power supply on J24, J25 expansion connectors
R17	IN	Enables the ICE NTRST input
R18	IN	Enables the ICE NRST input
R13	IN	Enables the use of the Y1 crystal. If an external clock has to be used, R13 and R15 must be unsoldered and R16/J16 fitted.
R15	IN	
R30	IN	Enables the use of the MN7 SDRAM device. Needs to be removed when ETM is used.(2)
R45	IN	Enables the use of the SERIAL EEPROM SCL (PB5)
R46	IN	Enables the use of the SERIAL EEPROM SDA (PB4)
R75	IN	Enables the use of the DBGU TXD signal (PC31)
R79	IN	Enables the use of the DBGU RXD signal (PC30)
R84	IN	Enables the use of the USB CNX detection (PA25)

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
R76	IN	Enables the use of the RS232 COM PORT TXD signal (PA26)
R78	IN	Enables the use of the RS232 COM PORT RTS signal (PA28)
R80	IN	Enables the use of the RS232 COM PORT RXD signal (PA27)
R82	IN	Enables the use of the RS232 COM PORT CTS signal (PA29)
R87	IN	Enables the use of the CAN BUS driver RS control signal (PA26)
R89	IN	Enables the use of the CAN BUS driver CANTXRT RTS signal (PA28)
R91	IN	Enables the use of the RS232 COM PORT RXD signal (PA27)
R93	IN	Enables the use of the RS232 COM PORT CTS signal (PA29)
R112	IN	Enables the use of interrupt ETHERNET PHY (PE31)
R126	IN	Enables the use of TOUCH SCREEN CONTROLLER (PB11_SPI0_NPCS3)
R127	IN	Enables the use of TOUCH SCREEN CONTROLLER BUSY signal (PA31)
R128	IN	Enables the use of TOUCH SCREEN CONTROLLER PENIRQ (PA15_IRQ1)
TP67	N.A	GND Test point
TP68	N.A	GND Test point
TP69	N.A	GND Test point
TP70	N.A	GND Test point
TP71	N.A	0 to 3.3V analog user's input
TP72	N.A	0 to 3.3V analog user's input
TP73	N.A	AGND of TP71
TP74	N.A	AGND of TP72

Note:
1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.
2. AT91SAM9263 ETM signals [TPK0 - TPK15] are multiplexed with EBI0 signals [EBI0_D16 - EBI0_D31]. AT91SAM9263-EK EBI0 signals [EBI0_D16 - EBI0_D31] are connected to an SDRAM device (part MN7).
   Having this SDRAM device enabled adds capacitance to the data line [EBI0_D16 - EBI0_D31], which leads to ETM data corruption.

   You need to remove the resistor R30 to release the EBI0_NCS1_SDCS signal and put the SDRAM I/Os [EBI0_D16 - EBI0_D31] in High-Z. Having these signals in High-Z removes the added capacitance; the ETM signals are no longer corrupted.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Power Supply
- AT91SAM9263
- EBI0 Memory
- EBI1 Memory
- Serial Memory
- Audio AC97
- Serial Interfaces
- Ethernet
- LCD and ISI
- Expansion




POWER SUPPLY

12VDC
- VDDBU
- POWERLED
- SHDN

USER'S INTERFACE
- USERLED1
- USERLED2
- RIGHTCLIC
- LEFTCLIC

01 - POWER SUPPLY

AC97

OUT / IN / MIC — AUDIO
- SYNC
- BITCLK
- SDATA_OUT
- SDATA_IN
- EXT_CLK
- RST#

06 - AUDIO

SERIAL INTERFACES

RS232
- DBGU: DTXD, DRXD
- COM0: TXD, RXD, RTS, CTS

USB
- DEVICE: USBCNX, DDM, DDP
- HOST A: HDMA, HDPA, ENA, FLGA
- HOST B: HDMB, HDPB, ENB, FLGB

CAN
- CANRS, CANRXEN, CANRX, CANTX

07 - COMMUNICATION

RMII ETHERNET

10/100 FAST ETHERNET
- TX_CLK
- TXD1, TXD0, TX_EN
- RXD1, RXD0, RX_DV, RX_ER
- MDC, MDIO, MDINTR
- NRST

08 - ETHERNET

LCD & CAMERA INTERFACE

LCD INTERFACE — 3.5" QVGA
- R[0..5], G[0..5], B[0..5]
- HSYNC, DCLK, DTMG
- VCTRL, PCI

TOUCH SCREEN CONTROLLER
- MOSI, MISO, SPCK, NPCS, IRQ, BUSY, RFTS

CAMERA INTERFACE — ISI
- ISI_D[0..11]
- ISI_MCK, ISI_VSYNC, ISI_HSYNC, ISI_PCK
- VDDISI
- SDA, SCL
- CTRL2, CTRL1

09 - LCD & CAMERA INTERFACE

EXPANSION CONNECTORS

PA[0..31], PB[0..31], PC[0..31], PD[0..31], PE[0..31], CLK16M, SIGI, SIGQ, RFTS

10 - EXPANSION CONNECTORS

AT91SAM9263_BGA324

VDDBU, SHDN, VDDISI, PA[0..31], PB[0..31], PC[0..31], PD[0..31], PE[0..31], DDM, DDP, HDMA, HDPA, HDMB, HDPB, PPS, CK16M, SIGI, SIGQ

02 - MICROCONTROLLER

EBI0 MEMORY

EBI0_D[0..31], EBI0_A[0..22]

SDRAM: RAS, CAS, SDA10, SDWE, SDCS, SDCK, SDCKE, NBS0–NBS3, BA0, BA1

NANFLASH: CLE, ALE, NANDOE, NANDWE, NANDCS, RDYBSY

NORFLASH: NCS, NWE, NRD, NRST

1.8" HDD: RESET-, CS0-, CS1-, DIOR-, DIOW-, INTRQ, IORDY

03 - EBI0 MEMORY

EBI1 MEMORY

EBI1_D[0..15], EBI1_A[0..21]

PSRAM: NCS, NWR, NOE, LB, UB

04 - EBI1 MEMORY

MCI & TWI

CARD READER — MMC SD/SDIO DATAFLASH: MCI0_CD, MCI0_WP, MCI0_DA0–MCI0_DA3, MCI0_CDA, MCI0_CK, SPI0_SPCK, CKSEL

CARD READER — MMC SD/SDIO: MCI1_CD, MCI1_WP, MCI1_DA0–MCI1_DA3, MCI1_CDA, MCI1_CK

SERIAL EEPROM: TWCK, TWD, SCL, SDA

05 - MCI & TWI

PIO USAGE

	PA[0..31]	PB[0..31]	PC[0..31]	PD[0..31]	PE[0..31]
0	SPI0_MISO PA0	PB0 AC97FS	PC0	PD0	PE0 ISI_D0
1	SPI0_MOSI PA1	PB1 AC97CK	PC1 LCDHSYNC	PD1	PE1 ISI_D1
2	PA2 SPI0_SPCK	PB2 AC97TX	PC2 LCDDOTCK	PD2 (INTRQ)	PE2 ISI_D2
3	PA3 MCI0_DA1	PB3 AC97RX	PC3 LCDDEN	PD3 (IORDY)	PE3 ISI_D3
4	PA4 MCI0_DA2	PB4 TWD	PC4 (RIGHTCLIC)	PD4	PE4 ISI_D4
5	PA5 MCI0_DA3	PB5 TWCK	PC5 (LEFTCLIC)	PD5	PE5 ISI_D5
6	PA6 MCI1_CK	PB6	PC6 LCDD2	PD6	PE6 ISI_D6
7	PA7 MCI1_CDA	PB7 PWM0	PC7 LCDD3	PD7	PE7 ISI_D7
8	PA8 MCI1_DA0	PB8 PWM1	PC8 LCDD4	PD8 EBI0_CFCE1	PE8 ISI_PCK
9	PA9 MCI1_DA1	PB9 LCDCC	PC9 LCDD5	PD9 EBI0_CFCE2	PE9 ISI_HSYNC
10	PA10 MCI1_DA2	PB10 PCK1	PC10 LCDD6	PD10	PE10 ISI_VSYNC
11	PA11 MCI1_DA3	PB11 SPI0_NPCS3	PC11 LCDD7	PD11	PE11 ISI_MCK
12	PA12 MCI0_CK	PB12	PC12 LCDD13	PD12	PE12 ISI_D8
13	PA13 CANTX	PB13	PC13	PD13	PE13 ISI_D9
14	PA14 CANRX	PB14	PC14 LCDD10	PD14	PE14 ISI_D10
15	PA15 IRQ1	PB15	PC15 LCDD11	PD15 (NANDCS)	PE15 ISI_D11
16	PA16 (CTRL1)	PB16	PC16 LCDD12	PD16	PE16 (MCI0_CD)
17	PA17 (CTRL2)	PB17	PC17 LCDD21	PD17	PE17 (MCI0_WP)
18	PA18 (CANRXEN)	PB18	PC18 LCDD14	PD18	PE18 (MCI1_CD)
19	PA19 (CANRS)	PB19	PC19 LCDD15	PD19	PE19 (MCI1_WP)
20	PA20 (FLGB)	PB20	PC20	PD20	PE20 (CKSEL)
21	PA21 (ENB)	PB21	PC21	PD21	PE21 ETXCK
22	PA22 (RDYBSY)	PB22	PC22 LCDD18	PD22	PE22
23	PA23 (FLGA)	PB23	PC23 LCDD19	PD23	PE23 ETX0
24	PA24 (ENA)	PB24	PC24 LCDD20	PD24	PE24 ETX1
25	PA25 (USBCNX)	PB25	PC25 ERXDV	PD25	PE25 ERX0
26	PA26 TXD0	PB26	PC26 LCDD22	PD26	PE26 ERX1
27	PA27 RXD0	PB27	PC27 LCDD23	PD27	PE27 ERXER
28	PA28 RTS0	PB28	PC28	PD28	PE28 ETXEN
29	PA29 CTS0	PB29	PC29 PWM2	PD29	PE29 EMDC
30	PA30 (PCI)	PB30	PC30 DRXD	PD30	PE30 EMDIO
31	PA31 (BUSY)	PB31	PC31 DTXD	PD31	PE31 (MDINTR)

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	10/10/06		

ATMEL ROUSSET

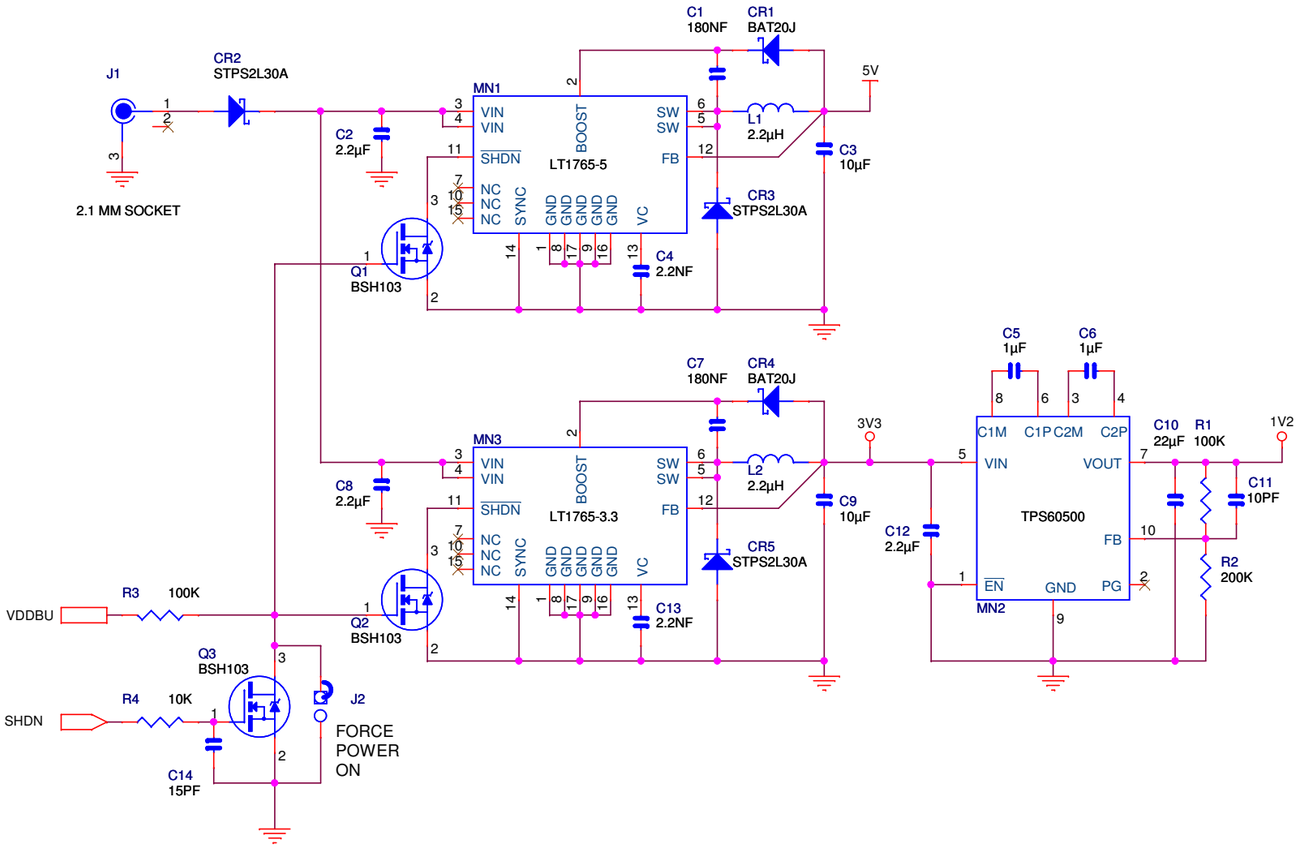
AT91SAM9263-EK

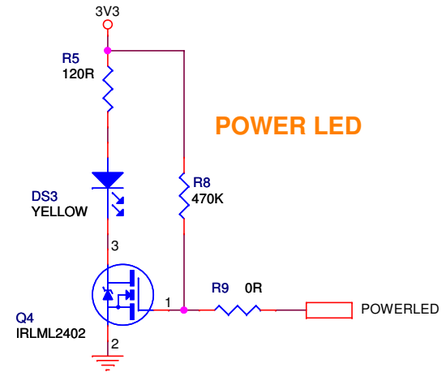
DIAGRAM

SCALE 1/1

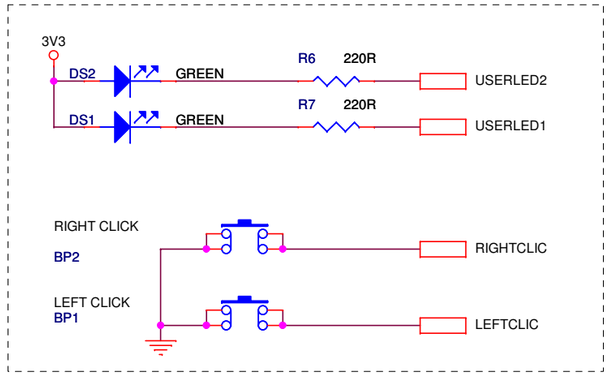
REV. A

SHEET 1/11





USER INTERFACE



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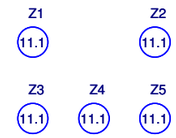
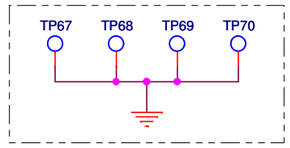


GND TEST POINT



ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	10/10/06		

AT91SAM9263-EK

POWER SUPPLY

SCALE 1/1

REV. A

SHEET 2/11

PA[0..31]

MN4A

PA0	N16	PA0/MCI0_DA0/SPI0_MISO
PA1	N15	PA1/MCI0_CDA/SPI0_MOSI
PA2	P15	PA2/SPI0_SPCK
PA3	P14	PA3/MCI0_DA1/SPI0_NPCS1
PA4	M15	PA4/MCI0_DA2/SPI0_NPCS2
PA5	M17	PA5/MCI0_DA3/SPI0_NPCS0
PA6	M14	PA6/MCI1_CK/PCK2
PA7	M16	PA7/MCI1_CDA
PA8	M18	PA8/MCI1_DA0
PA9	L15	PA9/MCI1_DA1
PA10	L17	PA10/MCI1_DA2
PA11	L18	PA11/MCI1_DA3
PA12	L16	PA12/MCI0_CK
PA13	L13	PA13/CANTX/PCK0
PA14	K14	PA14/CANRX/IRQ0
PA15	K15	PA15/TCLK2/IRQ1
PA16	P3	PA16/MCI0_CDB/EBI1_D16
PA17	U1	PA17/MCI0_DB0/EBI1_D17
PA18	R3	PA18/MCI0_DB1/EBI1_D18
PA19	T3	PA19/MCI0_DB2/EBI1_D19
PA20	U2	PA20/MCI0_DB3/EBI1_D20
PA21	T4	PA21/MCI1_CDB/EBI1_D21
PA22	V2	PA22/MCI1_DB0/EBI1_D22
PA23	U3	PA23/MCI1_DB1/EBI1_D23
PA24	U4	PA24/MCI1_DB2/EBI1_D24
PA25	R4	PA25/MCI1_DB3/EBI1_D25
PA26	T5	PA26/TXD0/EBI1_D26
PA27	V3	PA27/RXD0/EBI1_D27
PA28	U5	PA28/RTS0/EBI1_D28
PA29	V4	PA29/CTS0/EBI1_D29
PA30	R5	PA30/SCK0/EBI1_D30
PA31	T6	PA31/DMARQ0/EBI1_D31

MN4B

PB0/AC97FS/TF0	K17	PB0
PB1/AC97CK/TK0	K16	PB1
PB2/AC97TX/TD0	K18	PB2
BMS_PB3/AC97RX/RD0	K13	PB3
PB4/TWD/RK0	L14	PB4
PB5/TWCK/RF0	J15	PB5
PB6/TF1/DMARQ1	J16	PB6
PB7/TK1/PWM0	J17	PB7
PB8/TD1/PWM1	J18	PB8
PB9/RD1/LCDCC	J13	PB9
PB10/RK1/PCK1	J14	PB10
PB11/RF1/SPI0_NPCS3	J12	PB11
PB12/SPI1_MISO	H18	PB12
PB13/SPI1_MOSI	H15	PB13
PB14/SPI1_SPCK	H17	PB14
PB15/SPI1_NPCS0	H14	PB15
PB16/SPI1_NPCS1/PCK1	B17	PB16
PB17/SPI1_NPCS2/TIOA2	H13	PB17
PB18/SPI1_NPCS3/TIOB2	G18	PB18
PB19/LVRST	H12	PB19
PB20/CKSYNC	G14	PB20
PB21/PCTL0	G13	PB21
PB22/CKDAT	G17	PB22
PB23/GPSSYNC	G15	PB23
PB24/OTG_SE0_VM/DMARQ3	H16	PB24
PB25/OTG_DAT_VP	F15	PB25
PB26/OTGTP_OE	F14	PB26
PB27/OTGRCV/PWM2	F17	PB27
PB28/OTGSUSPEND/TCLK0	G16	PB28
PB29/OTGINT/PWM3	F16	PB29
PB30/OTGTWD	E15	PB30
PB31/OTGTWCK	E17	PB31

PB[0..31]

PB3

R134 4.7K

J5-6

R135 4.7K

BOOT MODE SELECT
Opened = Internal ROM BOOT
Closed = NCS0

PC[0..31]

MN4C

PC0	E16	PC0/LCDVSYNC
PC1	D17	PC1/LCDHSYNC
PC2	D16	PC2/LCDDOTCK
PC3	C15	PC3/LCDDEN/PWM1
PC4	E14	PC4/LCDD0/LCDD3
PC5	B16	PC5/LCDD1/LCDD4
PC6	D13	PC6/LCDD2/LCDD5
PC7	B15	PC7/LCDD3/LCDD6
PC8	C14	PC8/LCDD4/LCDD7
PC9	B14	PC9/LCDD5/LCDD10
PC10	D15	PC10/LCDD6/LCDD11
PC11	E13	PC11/LCDD7/LCDD12
PC12	A15	PC12/LCDD8/LCDD13
PC13	F13	PC13/LCDD9/LCDD14
PC14	C13	PC14/LCDD10/LCDD15
PC15	E12	PC15/LCDD11/LCDD19
PC16	D14	PC16/LCDD12/LCDD20
PC17	B13	PC17/LCDD13/LCDD21
PC18	F12	PC18/LCDD14/LCDD22
PC19	A14	PC19/LCDD15/LCDD23
PC20	D12	PC20/LCDD16/E_TX2
PC21	B12	PC21/LCDD17/E_TX3
PC22	E11	PC22/LCDD18/E_RX2
PC23	C12	PC23/LCDD19/E_RX3
PC24	A13	PC24/LCDD20/E_TXER
PC25	D11	PC25/LCDD21/E_RXDV
PC26	A12	PC26/LCDD22/E_COL
PC27	F11	PC27/LCDD23/E_RXCK
PC28	B11	PC28/PWM0/TCLK1
PC29	C11	PC29/PCK0/PWM2
PC30	A11	PC30/DRXD
PC31	E10	PC31/DTXD

MN4D

PD0/TXD1/SPI0_NPCS2	B10	PD0
PD1/RXD1/SPI0_NPCS3	D10	PD1
PD2/TXD2/SPI1_NPCS2	C10	PD2
PD3/RXD2/SPI1_NPCS3	F10	PD3
PD4/FIQ/DMARQ2	A10	PD4
PD5/EBI0_NWAIT/RTS2	G5	PD5
PD6/EBI0_NCS4/CFCS0/CTS2	G3	PD6
PD7/EBI0_NCS5/CFCS1/RTS1	F1	PD7
PD8/EBI0_CFCE1/CTS1	G6	PD8
PD9/EBI0_CFCE2/SCK2	H4	PD9
PD10/SCK1	G7	PD10
PD11/EBI0_NCS2/TSYNC	H5	TSYNC
PD12/EBI0_A23/TCLK	G2	TCLK
PD13/EBI0_A24/TPS0	H2	TPS0
PD14/EBI0_A25_CFRNW/TPS1	H6	TPS1
PD15/EBI0_NCS3/NANDCS/TPS2	H3	TPS2
PD16/EBI0_D16/TPK0	H7	TPK0
PD17/EBI0_D17/TPK1	G1	TPK1
PD18/EBI0_D18/TPK2	J5	TPK2
PD19/EBI0_D19/TPK3	J4	TPK3
PD20/EBI0_D20/TPK4	J8	TPK4
PD21/EBI0_D21/TPK5	J7	TPK5
PD22/EBI0_D22/TPK6	J3	TPK6
PD23/EBI0_D23/TPK7	J6	TPK7
PD24/EBI0_D24/TPK8	H1	TPK8
PD25/EBI0_D25/TPK9	K8	TPK9
PD26/EBI0_D26/TPK10	J2	TPK10
PD27/EBI0_D27/TPK11	K5	TPK11
PD28/EBI0_D28/TPK12	K2	TPK12
PD29/EBI0_D29/TPK13	K7	TPK13
PD30/EBI0_D30/TPK14	J1	TPK14
PD31/EBI0_D31/TPK15	K6	TPK15

PD[0..31]

RR3 0R
R139 0R
RR4 0R
RR5 0R
RR6 0R
RR7 0R

PE[0..31]

MN4E

PE0	K3	PE0/ISI_D0/DRFIN0
PE1	K4	PE1/ISI_D1/DRFIN1
PE2	L6	PE2/ISI_D2/DRFIN2
PE3	L7	PE3/ISI_D3/DRFIN3
PE4	L2	PE4/ISI_D4/DRFIN4
PE5	L5	PE5/ISI_D5/DRFIN5
PE6	K1	PE6/ISI_D6/DRFIN6
PE7	L4	PE7/ISI_D7/DRFIN7
PE8	M7	PE8/ISI_PCK/TIOA1
PE9	L3	PE9/ISI_HSYNC/TIOB1
PE10	L1	PE10/ISI_VSYNC/PWM3
PE11	M4	PE11/ISI_MCK/PCK3
PE12	M6	PE12/KBDR0/ISI_D8
PE13	M5	PE13/KBDR1/ISI_D9
PE14	M2	PE14/KBDR2/ISI_D10
PE15	M3	PE15/KBDR3/ISI_D11
PE16	N6	PE16/KBDPWR
PE17	N5	PE17/KBDC0
PE18	M1	PE18/KBDC1/TIOA0
PE19	N3	PE19/KBDC2/TIOB0
PE20	P6	PE20/KBDC3/EBI1_NWAIT
PE21	V13	PE21/E_TXCK/EBI1_NANDWE
PE22	U13	PE22/E_CRS/EBI1_NCS2/NANDCS
PE23	T13	PE23/E_TX0/EBI1_NANDOE
PE24	V14	PE24/E_TX1/EBI1_NWR3/NBS3/CFIOW
PE25	T14	PE25/E_RX0/EBI1_NCS1/SDCS
PE26	R14	PE26/E_RX1
PE27	U14	PE27/E_RXER/EBI1_SDCKE
PE28	P16	PE28/E_TXEN/EBI1_RAS
PE29	T15	PE29/E_MDC/EBI1_CAS
PE30	R16	PE30/E_MDIO/EBI1_SDWE
PE31	T16	PE31/E_F100/EBI1_SDA10

ICE INTERFACE

J7

RR1 100K

R17 0R

R18 0R

NTRST	U16	NTRST
TDI	P17	TDI
TMS	N17	TMS
TCK	R17	TCK
RTCK	U15	RTCK
TDO	N18	TDO
JTAGSEL	P5	S1
NRST	V15	NRST

J6 NOT POPULATED

SMB MALE

R14 NOT POPULATED

R16 NOT POPULATED

R19 1K

BP3 NRST

BP4 WAKE UP

R20 100K

SHDN

R21 10K

EBI0_D[0..31]

MN4F

EBI0_D0	C2	EBI0_D0
EBI0_D1	D4	EBI0_D1
EBI0_D2	A1	EBI0_D2
EBI0_D3	D2	EBI0_D3
EBI0_D4	B1	EBI0_D4
EBI0_D5	E3	EBI0_D5
EBI0_D6	C1	EBI0_D6
EBI0_D7	E2	EBI0_D7
EBI0_D8	E4	EBI0_D8
EBI0_D9	F3	EBI0_D9
EBI0_D10	D1	EBI0_D10
EBI0_D11	F4	EBI0_D11
EBI0_D12	F5	EBI0_D12
EBI0_D13	F2	EBI0_D13
EBI0_D14	G4	EBI0_D14
EBI0_D15	E1	EBI0_D15

EBI0_A[0..22]

EBI0_A0	E9	EBI0_NBS0/A0
EBI0_A1	A9	EBI0_NBS2/NWR2/A1
EBI0_A2	D9	EBI0_A2
EBI0_A3	C9	EBI0_A3
EBI0_A4	B9	EBI0_A4
EBI0_A5	A8	EBI0_A5
EBI0_A6	F9	EBI0_A6
EBI0_A7	B8	EBI0_A7
EBI0_A8	C8	EBI0_A8
EBI0_A9	D8	EBI0_A9
EBI0_A10	A7	EBI0_A10
EBI0_A11	A6	EBI0_A11
EBI0_A12	F8	EBI0_A12
EBI0_A13	C7	EBI0_A13
EBI0_A14	E7	EBI0_A14
EBI0_A15	B7	EBI0_A15
EBI0_A16	F7	EBI0_BA0/A16
EBI0_A17	D6	EBI0_BA1/A17
EBI0_A18	D7	EBI0_A18
EBI0_A19	A5	EBI0_A19
EBI0_A20	D5	EBI0_A20
EBI0_A21	C6	EBI0_A21
EBI0_A22	B6	EBI0_A22

EBI0_RAS	B4	EBI0_RAS
EBI0_CAS	B3	EBI0_CAS
EBI0_SDWE	C4	EBI0_SDWE
EBI0_SDA10	E8	EBI0_SDA10
EBI0_SDCKE	A2	EBI0_SDCKE
EBI0_SDCK	C5	EBI0_SDCK
EBI0_NCS0	F6	EBI0_NCS0
EBI0_NCS1/SDCS	A4	EBI0_NCS1/SDCS
EBI0_NRD/CFOE	E6	EBI0_NRD/CFOE
EBI0_NWE/NWR0/CFWE	A3	EBI0_NWE/NWR0/CFWE
EBI0_NBS1/NW1/CFIOR	E5	EBI0_NBS1/NWR1/CFIOR
EBI0_NBS3/NW3/CFIOW	B5	EBI0_NBS3/NWR3/CFIOW
EBI0_NANDOE	B2	EBI0_NANDOE
EBI0_NANDWE	C3	EBI0_NANDWE

RESERVED FOR FUTURE USE

PPS	G9	PPS
SIGI	V16	RFIN1
SIGQ	V17	RFIN2
CK16M		

MN4H

HDPB	C18	HDPB
HDMB	D18	HDMB
HDPA	E18	HDPA
HDMA	F18	HDMA
DDP	A18	DDP
DDM	B18	DDM
	P18	PLLRCB
	U18	PLLRCA
	R18	XOUT
	T18	XIN
	R1	XOUT32
	P1	XIN32
	U16	NTRST
	P17	TDI
	N17	TMS
	R17	TCK
	U15	RTCK
	N18	TDO
	P5	JTAGSEL
	V15	NRST
	P2	SHDN
	P4	WKUP
	D3	NC
	N1	NC
	N2	NC
	N4	NC
	R2	TST

C22 4.7NF
C24 470 pF
C25 10NF
C26 1NF
C28 22PF
C31 22PF
C33 15PF
C36 15PF

R11 1,96K 1%
R12 1.5K
R13 0R
R15 0R

Y1 16.36766MHz
Y2 32.768 kHz

EBI1_D[0..15]

EBI1_A[0..21]

MN4G

EBI1_D0	T10	EBI1_D0
EBI1_D1	R10	EBI1_D1
EBI1_D2	N10	EBI1_D2
EBI1_D3	U11	EBI1_D3
EBI1_D4	P12	EBI1_D4
EBI1_D5	V11	EBI1_D5
EBI1_D6	N11	EBI1_D6
EBI1_D7	T11	EBI1_D7
EBI1_D8	R11	EBI1_D8
EBI1_D9	N12	EBI1_D9
EBI1_D10	P13	EBI1_D10
EBI1_D11	V12	EBI1_D11
EBI1_D12	R12	EBI1_D12
EBI1_D13	U12	EBI1_D13
EBI1_D14	T12	EBI1_D14
EBI1_D15	R13	EBI1_D15
EBI1_A0	U6	EBI1_NBS0/A0
EBI1_A1	V5	EBI1_NWR2/A1
EBI1_A2	R6	EBI1_A2
EBI1_A3	V6	EBI1_A3
EBI1_A4	P8	EBI1_A4
EBI1_A5	U7	EBI1_A5
EBI1_A6	N7	EBI1_A6
EBI1_A7	T7	EBI1_A7
EBI1_A8	P7	EBI1_A8
EBI1_A9	V7	EBI1_A9
EBI1_A10	U8	EBI1_A10
EBI1_A11	N8	EBI1_A11
EBI1_A12	T8	EBI1_A12
EBI1_A13	R8	EBI1_A13
EBI1_A14	R7	EBI1_A14
EBI1_A15	V8	EBI1_A15
EBI1_A16	U9	EBI1_A16
EBI1_A17	R9	EBI1_A17
EBI1_A18	T9	EBI1_A18
EBI1_A19	P9	EBI1_A19
EBI1_A20	V9	EBI1_A20
EBI1_A21	M9	EBI1_A21
EBI1_A22	N9	NOT USED

EBI1_SDCK	R15	EBI1_SDCK
EBI1_NCS0	P10	EBI1_NCS0
EBI1_NRD/CFOE	U10	EBI1_NRD/CFOE
EBI1_NWE/NWR0/CFWE	P11	EBI1_NWE/NWR0/CFWE
EBI1_NBS1/NWR1/CFIOR	V10	EBI1_NBS1/NW1/CFIOR

ETM TRACE PORT

TPS0	PIPESTAT[0]	38	37	TRACEPKT[8]	TPK8
TPS1	PIPESTAT[1]	36	35	TRACEPKT[9]	TPK9
TPS2	PIPESTAT[2]	34	33	TRACEPKT[10]	TPK10
TSYNC	TRACESYNC	32	31	TRACEPKT[11]	TPK11
TPK0	TRACEPKT[0]	30	29	TRACEPKT[12]	TPK12
TPK1	TRACEPKT[1]	28	27	TRACEPKT[13]	TPK13
TPK2	TRACEPKT[2]	26	25	TRACEPKT[14]	TPK14
TPK3	TRACEPKT[3]	24	23	TRACEPKT[15]	TPK15
TPK4	TRACEPKT[4]	22	21		NTRST
TPK5	TRACEPKT[5]	20	19		TDI
TPK6	TRACEPKT[6]	18	17		TMS
TPK7	TRACEPKT[7]	16	15		TCK
	VSUPPLY	14	13		RTCK
	EXTTRIG	12	11		TDO
	TRACECLK	10	9		NRST
		8	7	DBGRQ	
		6	5	GND	
		4	3		
		2	1		

3V3 R136 10K

TCLK R137 0R

C160 100NF

R138 10K

G1 G2 G3 G4 G5 J28

3V3 CR6 MMBD1704A J3

J4-1 VDDBU

MN5 R1100D121C

C16 100NF

OUT GND VDD

CR1225 3V Z7

1K R10

J4-2 1V2

J5-1 3V3

J5-2 3V3

J5-3 3V3 VDDISI

J5-4 3V3

J5-5 3V3

VDDBU	M8	C15 100NF
GNDBU	L12	
VDDCORE	V1	C17 100NF
VDDCORE	H10	C18 100NF
VDDCORE	A16	C19 100NF
VDDPLLB	V18	C20 100NF
VDDPLLA	U17	C21 100NF
VDDOSC	T1	C23 100NF
GNDPLLB	T17	
GNDPLLA	N14	
VDDIOP0	L11	C27 100NF
VDDIOP0	C17	C29 100NF
VDDIOP0	A17	C30 100NF
VDDIOP1	L8	C32 100NF
VDDIOM0	L10	C34 100NF
VDDIOM0	K12	C35 100NF
VDDIOM0	K10	C37 100NF
VDDIOM0	H8	C38 100NF
VDDIOM1	T2	C39 100NF
VDDIOM1	M13	C40 100NF
VDDIOM1	M10	C41 100NF
VDDIOM1	L9	C42 100NF

GND	C8	G10	G11	G12	H9	H11
GND	J9	J10	J11	K9	K11	M11
GND	M12	N13				

ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	10/10/06		

AT91SAM9263-EK

AT91SAM9263

SCALE 1/1

REV. A

SHEET 3/11

SDRAM

A[0..22]
D[0..31]

MN6 MT48LC16M16A2 — 256 Mbits

MN7 MT48LC16M16A2 — 256 Mbits

3V3
C43 100NF
C45 100NF
C47 100NF
C49 100NF
C51 100NF
C53 100NF
C55 100NF
C44 100NF
C46 100NF
C48 100NF
C50 100NF
C52 100NF
C54 100NF
C56 100NF

SDA10 BA0 BA1 A13 A14 SDCKE SDCK NBS0 NBS1 CAS RAS SDWE

SDCS — R26 0R — R25 470K

NBS2 NBS3

R27 470K — R30 0R

NORFLASH

MN8 AT49BV642D — NOT POPULATED

P15 R22 0R A20
R23 NOT POPULATED
P9 R24 0R A22

NRST NWE NRD NCS

R28 0R — R29 470K — 3V3

C57 100NF
C58 100NF

NANDFLASH

DUAL FOOTPRINT

MN21A 16-bit bus width
MN21B 8-bit bus width

CLE ALE NANDOE NANDWE NANDCS RDYBSY

R31 0R
R32 0R
R36 0R
R33 470K
R34 0R
R35 1K
R37 470K

S2

C60 100NF
C59 100NF

NOT POPULATED

IDE CONNECTOR

J8 — IDE ATA-6

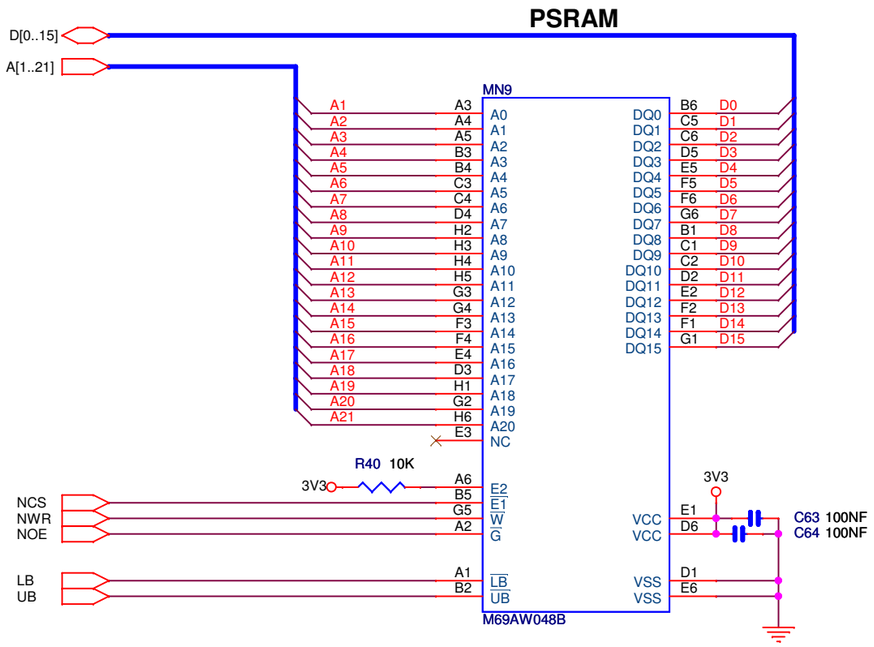
RESET- DIOW- DIOR- IORDY INTRQ CS0- CS1-

R38 10K
R39 10K

C62 10µF 10V
C61 100NF

A	INIT EDIT	JPG	10/10/06			
REV	MODIF.	DES.	DATE	VER.	DATE	
AT91SAM9263-EK				REV.	SHEET	
EBI0 MEMORY	SCALE 1/1			A	4/11	

PSRAM

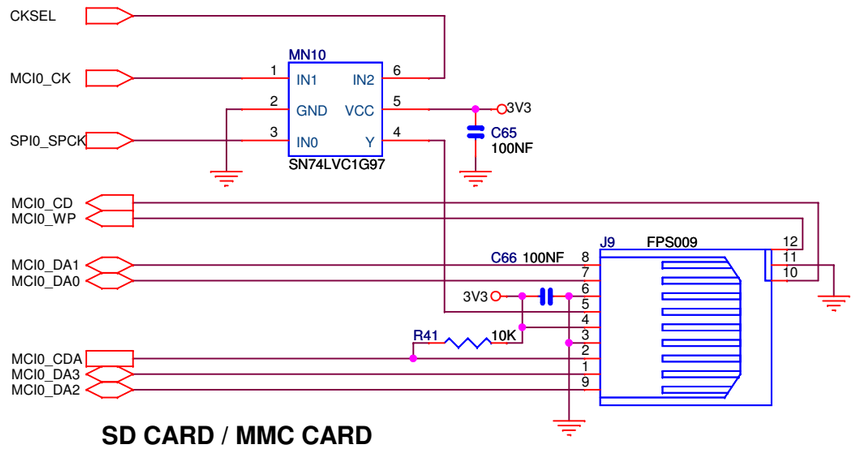


A	INIT EDIT	JPG	10/10/06			
REV	MODIF.	DES.	DATE	VER.	DATE	
				REV.	SHEET	
				A	5/11	

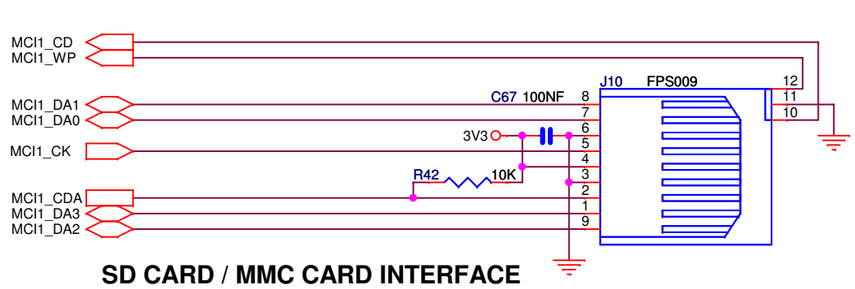
AT91SAM9263-EK

EBI1 MEMORY

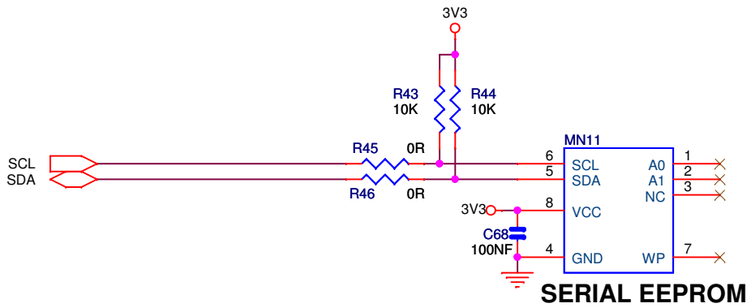
SCALE 1/1



SD CARD / MMC CARD
DATAFLASH CARD INTERFACE



SD CARD / MMC CARD INTERFACE



SERIAL EEPROM

A	INIT EDIT	JPG	10/10/06		
REV.	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9263-EK

SERIAL MEMORY

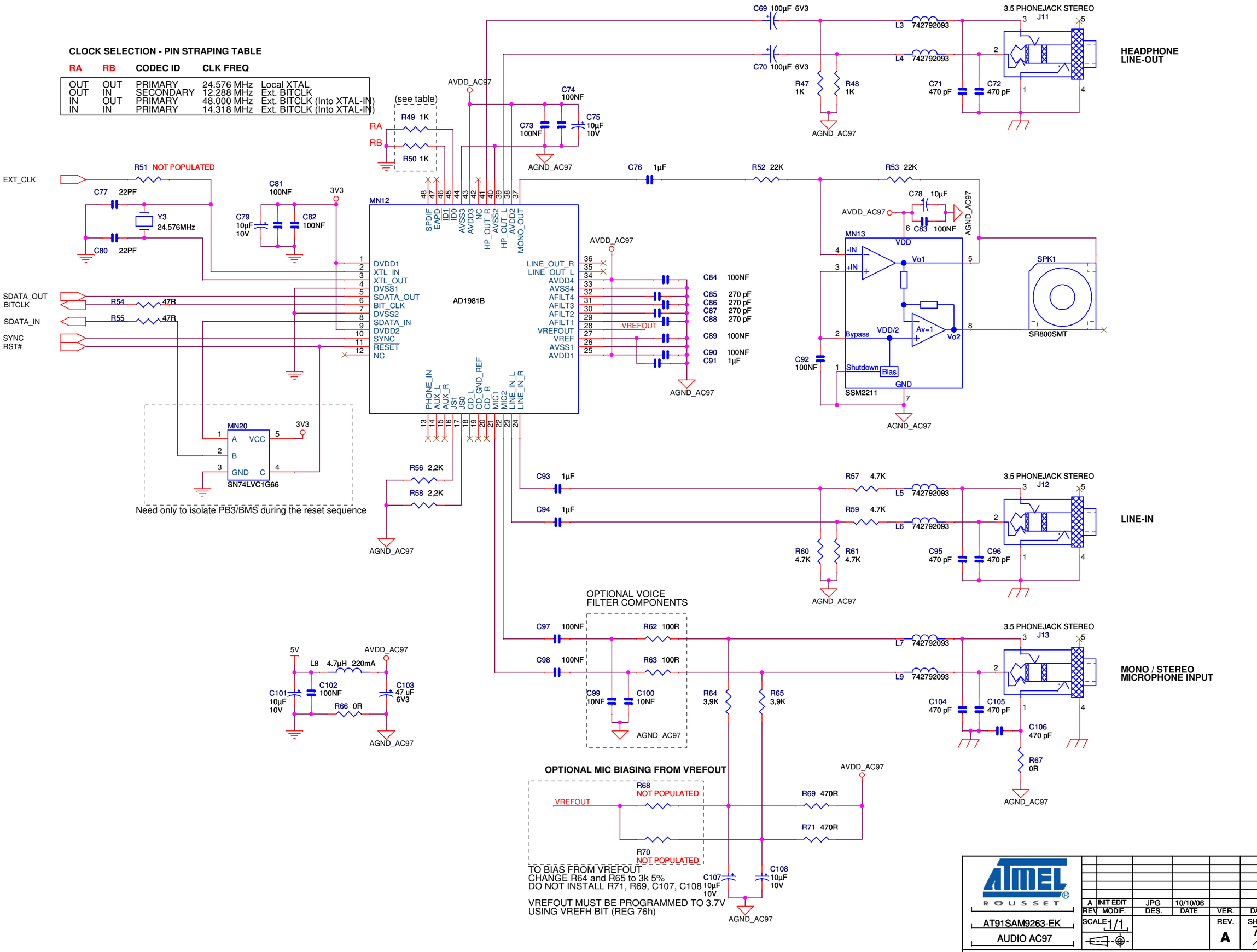
SCALE 1/1

REV. A

SHEET 6/11

CLOCK SELECTION - PIN STRAPING TABLE

RA	RB	CODEC ID	CLK FREQ	
OUT	OUT	PRIMARY	24.576 MHz	Local XTAL
OUT	IN	SECONDARY	12.288 MHz	Ext. BITCLK
IN	OUT	PRIMARY	48.000 MHz	Ext. BITCLK (Into XTAL-IN)
IN	IN	PRIMARY	14.318 MHz	Ext. BITCLK (Into XTAL-IN)



REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	10/10/06		

AT91SAM9263-EK

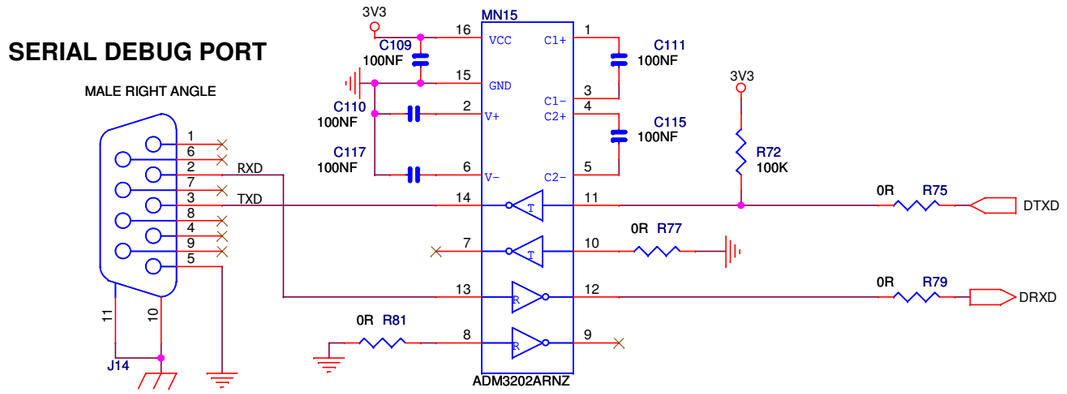
AUDIO AC97

SCALE 1/1

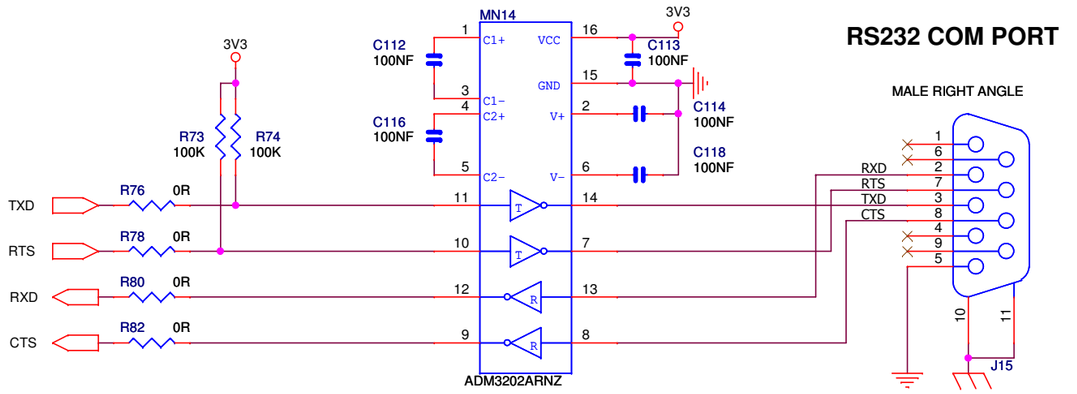
REV. A

SHEET 7/11

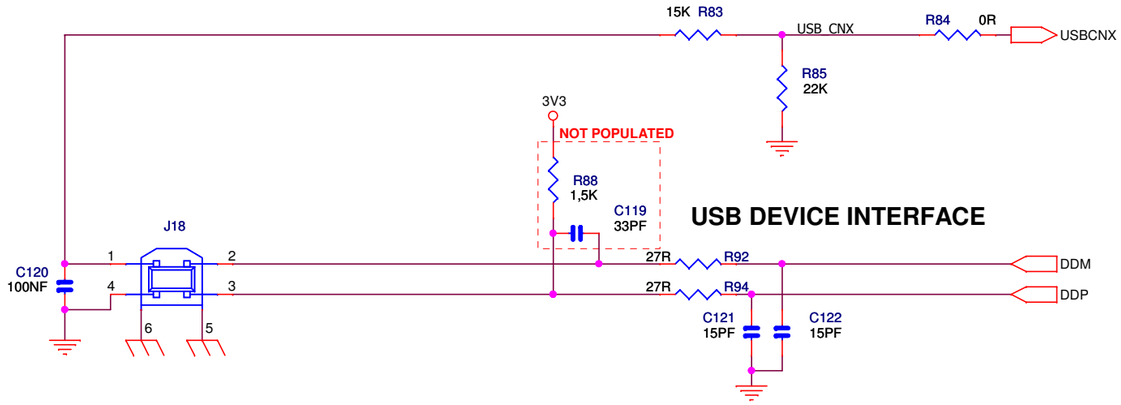
SERIAL DEBUG PORT



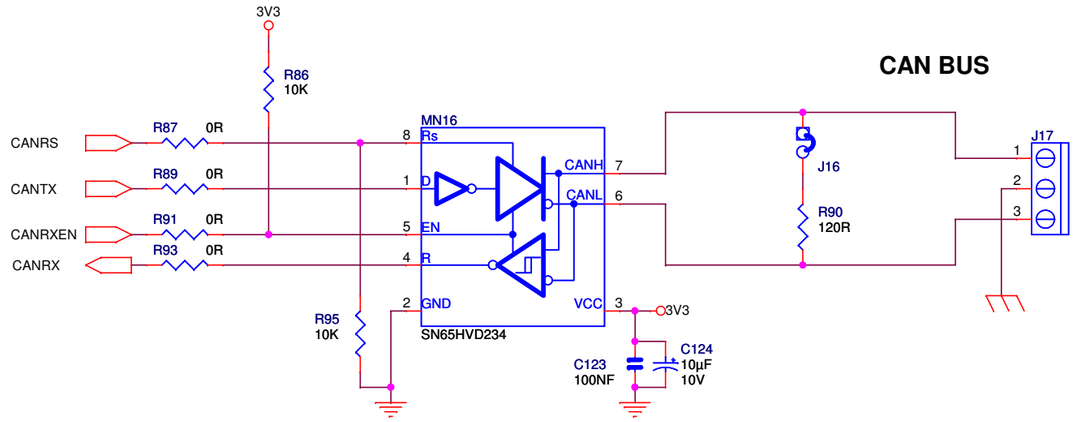
RS232 COM PORT



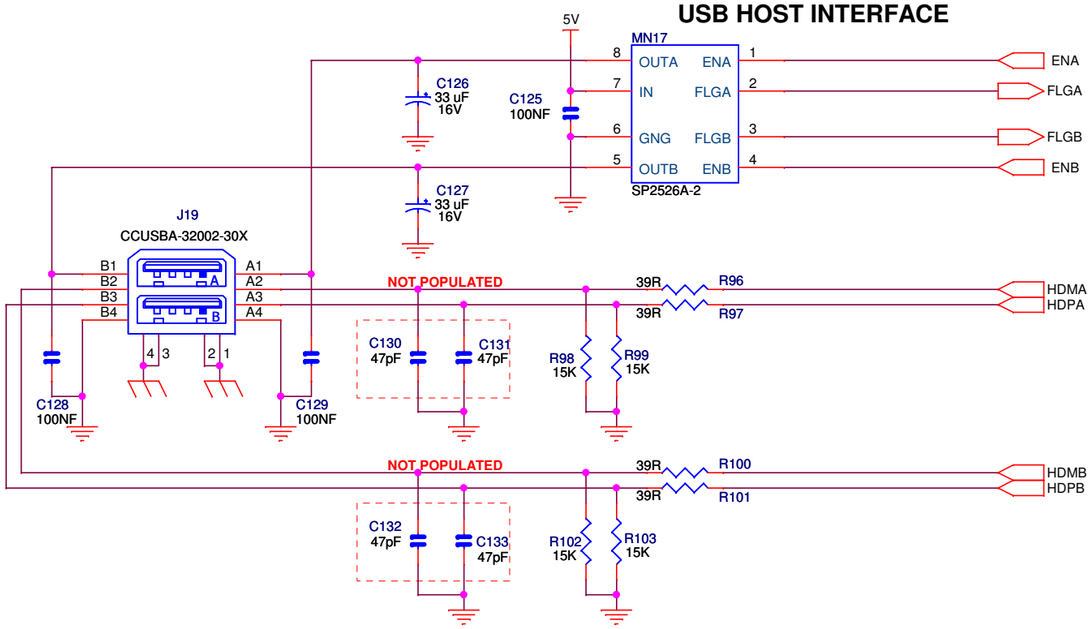
USB DEVICE INTERFACE



CAN BUS



USB HOST INTERFACE



A	INIT EDIT	JPG	10/10/06		
REV	MODIF.	DES.	DATE	VER.	DATE

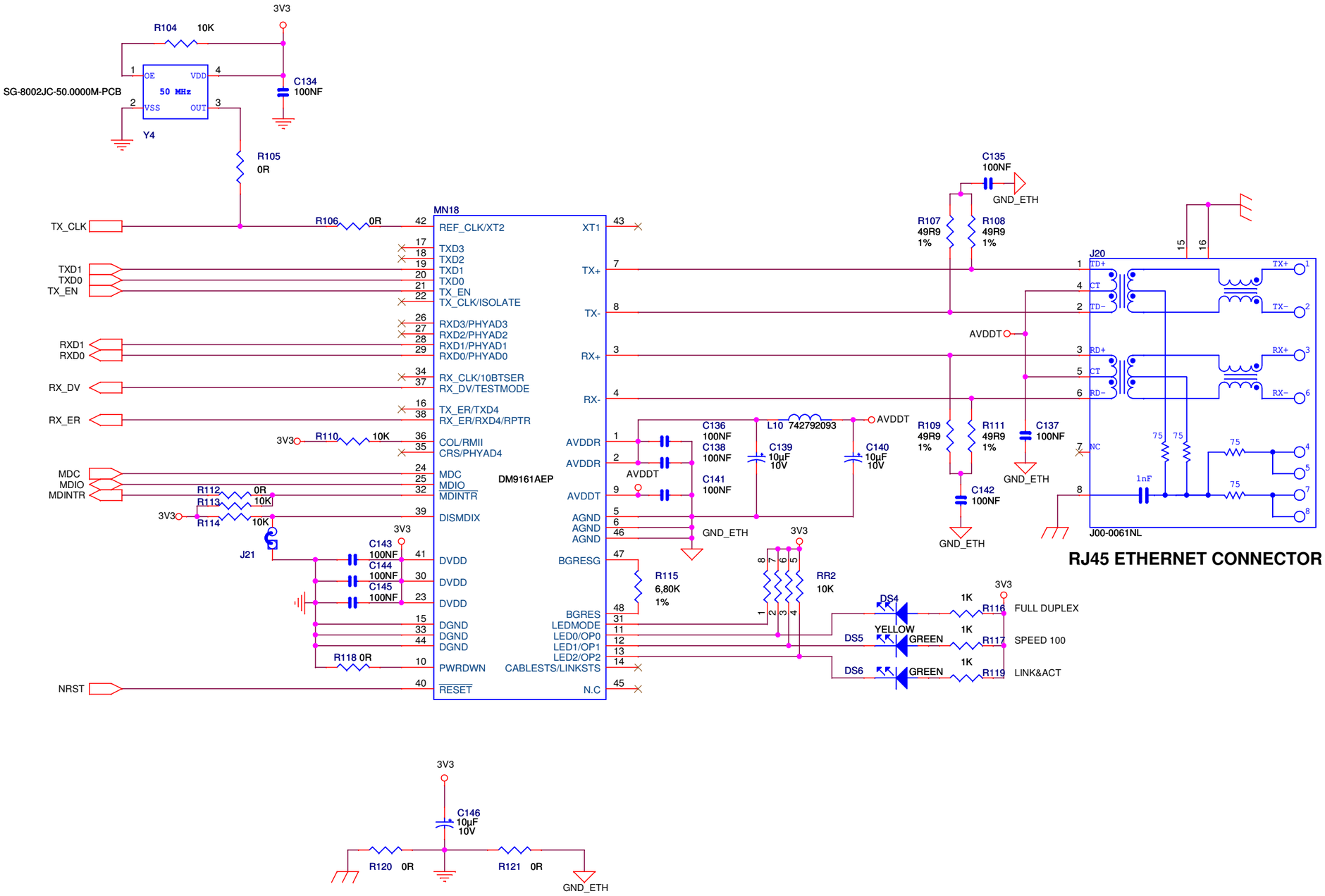
AT91SAM9263-EK

SERIAL INTERFACES

SCALE 1/1

REV. A

SHEET 8/11



RJ45 ETHERNET CONNECTOR

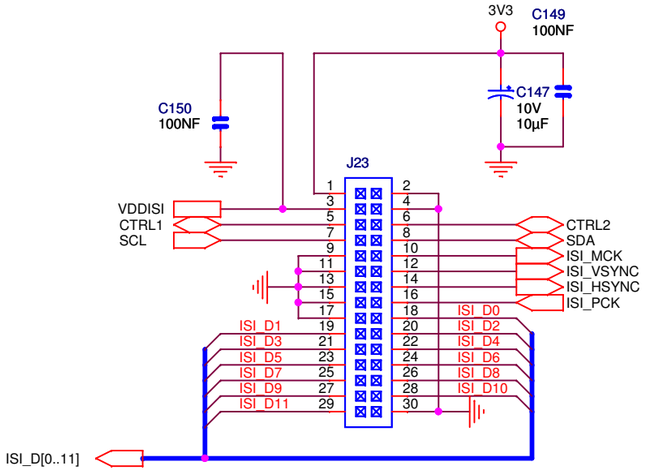
A	INIT EDIT	JPG	10/10/06		
REV	MODIF.	DES.	DATE	VER.	DATE
				REV. A	SHEET 9/11

AT91SAM9263-EK

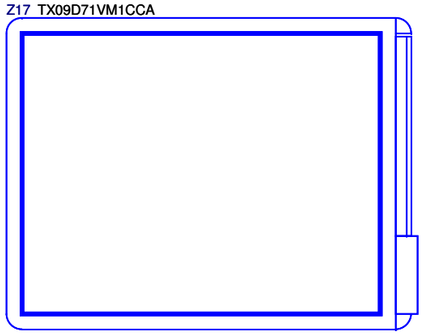
ETHERNET

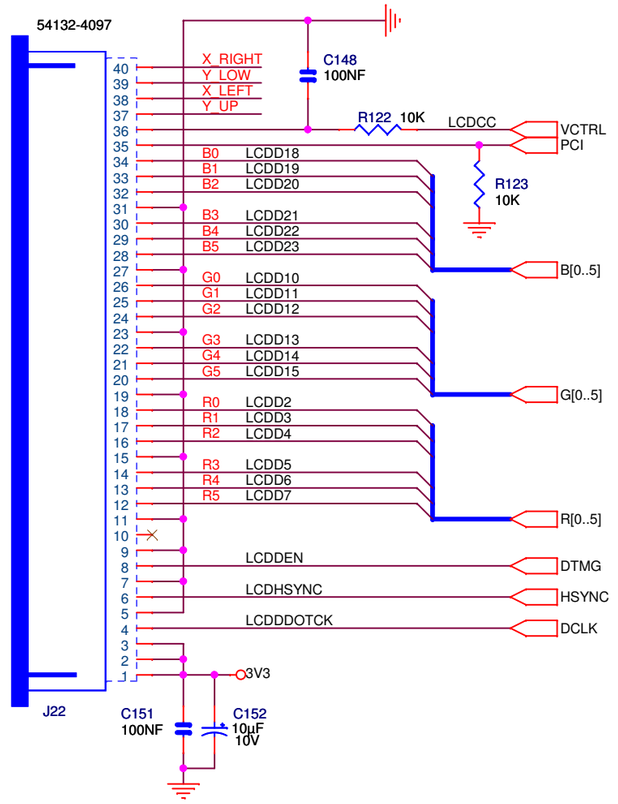
SCALE 1/1

IMAGE SENSOR CONNECTOR

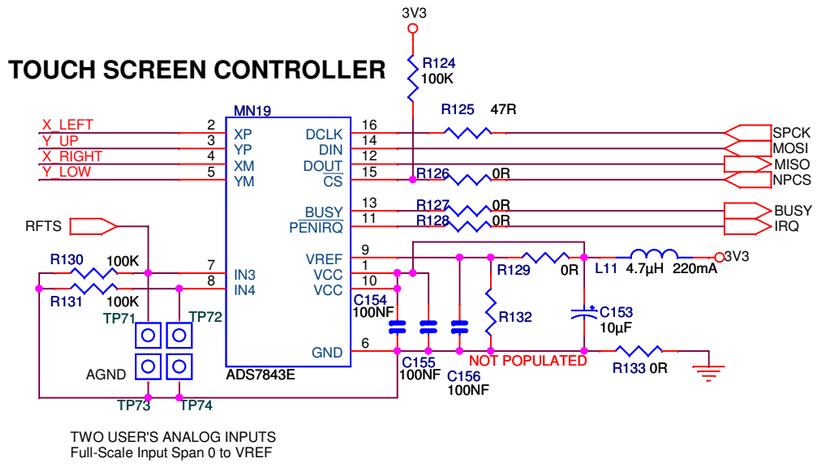


1/4 VGA TFT LCD DISPLAY





TOUCH SCREEN CONTROLLER



TWO USER'S ANALOG INPUTS
Full-Scale Input Span 0 to VREF

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	10/10/06		

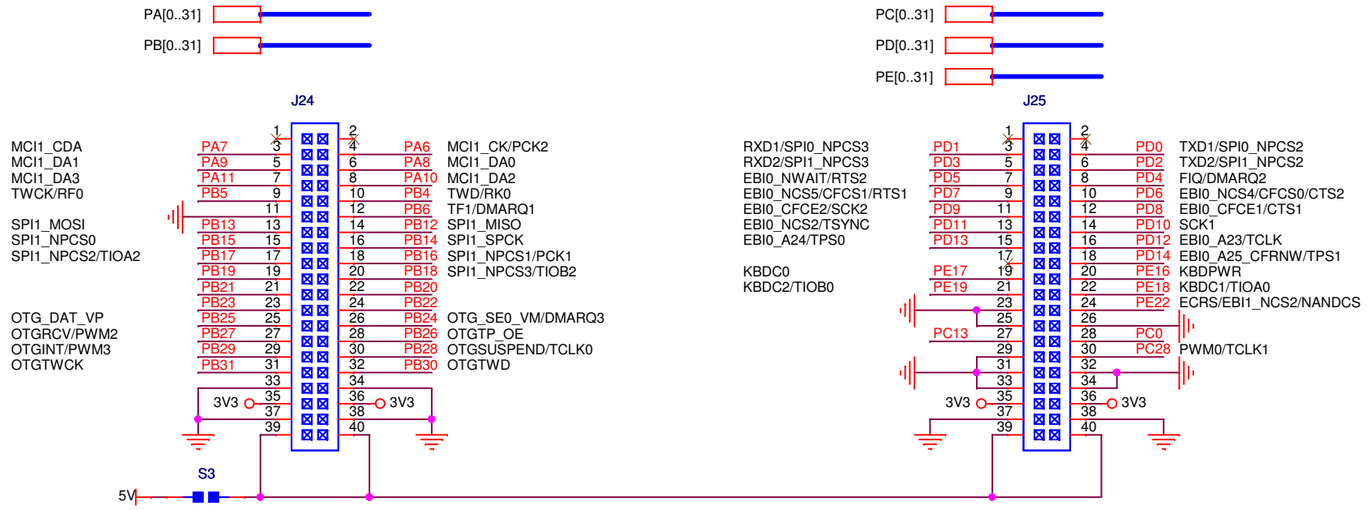
AT91SAM9263-EK

LCD & ISI

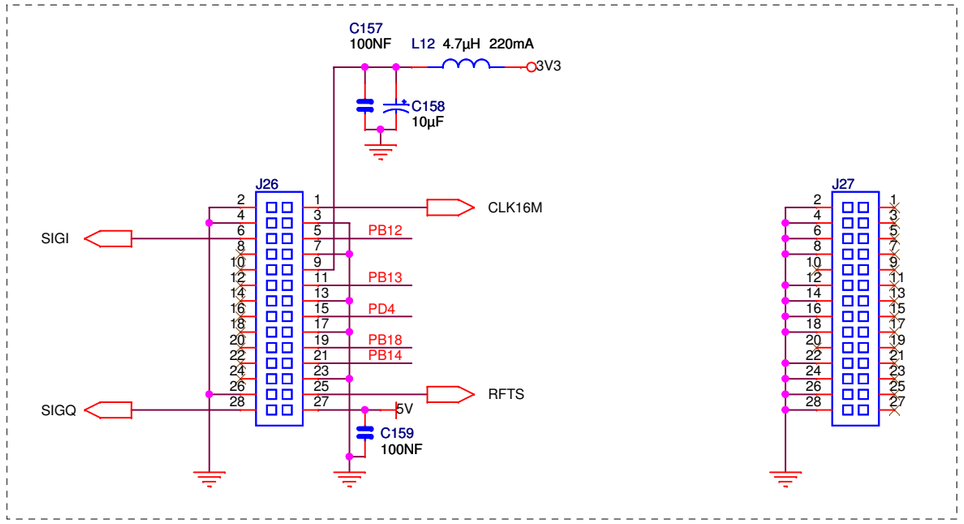
SCALE 1/1

REV. A

SHEET 10/11



RESERVED - NOT POPULATED



A	INIT EDIT	JPG	10/10/06		
REV	MODIF.	DES.	DATE	VER.	DATE

AT91SAM9263-EK

EXPANSION

SCALE 1/1

REV. A

SHEET 11/11

Section 6

Warning

6.1 BMS Signal Sampling

The following behavior and its consequences are related to an AT91SAM9263 device issue described in the Errata section of the AT91SAM9263 datasheet (“BMS: BMS does not have correct state”). The text below is a reminder of this issue and a Workaround proposal at the board level.

Description

The BMS signal, which is multiplexed with the PB3/AC97RX PIO needs to be sampled at a High Level for the AT91SAM9263 microcontroller to boot out of the internal ROM.

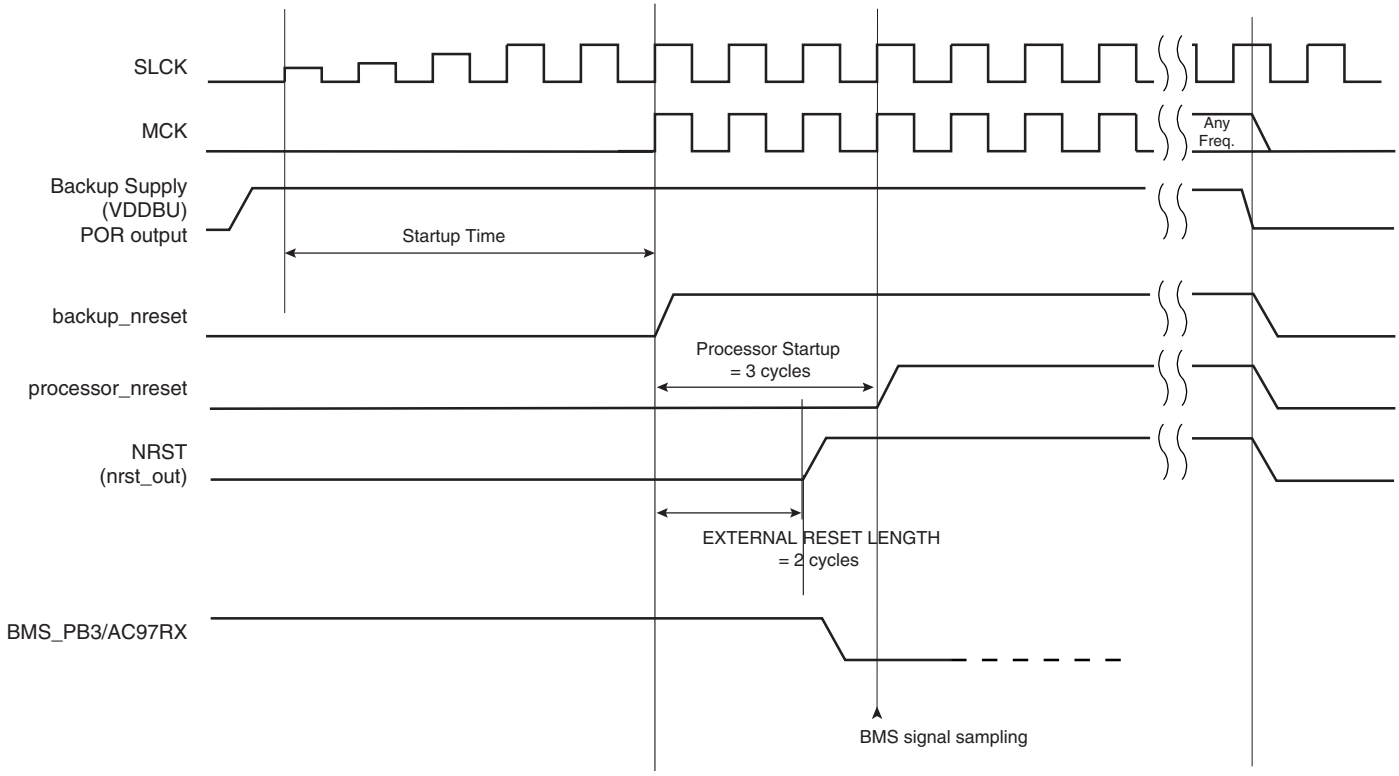
At power up, the on-board AC97 device negates its “SDATA_IN” output pin and due to this fact, the BMS_PB3/AC97RX pin needs to be isolated during the reset phase.

The MN20 gate, controlled by the NRST signal, achieves this, but with the default ERSTL value in the reset controller (refer to the RSTC section in the AT91SAM9263 datasheet for more details), when the VDDBU power supply is applied for more than 1.2 seconds before the VDDCORE power supply, the AT91SAM9263 microcontroller samples the BMS signal one Slow Clock (SLCK) cycle after the NRST signal rising (See Figure 6-1).

As a result, the BMS signal is sampled at a Low Level and the AT91SAM9263 boots out of the external EBI device connected to NCS0.

Warning

Figure 6-1. BMS Signal Sampling



Workaround:

At the first VDDBU power up or if this power supply has been shut down (J4-1 opened (VDDBU/VDDBACKUP Jumper) or the CR1225 battery cell (J3) removed or changed), the following power-up sequence has to be applied in order to boot out of the internal ROM:

1. Close J2 to force power on
2. Open J5 (Boot Mode Select Jumper)
3. Power on the board
4. Remove and replace J4-1 (VDDBU/VDDBACKUP Jumper)

Section 7

Errata

7.1 JTAGSEL S1 Footprint Selector

The S1 footprint must never be shorted to select a JTAG mode, else the chip can be damaged.

By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode). To select the JTAG mode, connect the JTAGSEL input pin to VDDBU power.

7.2 PIO Usage

PC20 and PC21 are not routed on the PCB. As a result, these signals are inaccessible.

7.3 TWI Line Pull-Ups for Fast Mode Operation

In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R43 and R44 should be replaced by smaller values (e.g., 2.2 KΩ).

Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).

Section 8

Revision History

8.1 Revision History

Table 8-1.

Document	Comments	Change Request Ref.
6279A	First issue.	
6279B	Added errata Section 7.3, ” TWI line pullups for Fast Mode operation”	4087
6279C	Updated Section 1.2, “AT91SAM9263-EK Evaluation Board” . Deleted some Peripheral A labels from Table 3-2, “PIO Controller B,” on page 3-8 and Table 3-5, “PIO Controller E,” on page 3-11 and some Peripheral B labels from Table 3-5, “PIO Controller E,” on page 3-11. New schematic Sheet 3/11 on AT91SAM9263-EK. Added Section 6.	4506 4404 4371
6279D	Issue not applicable: GPS signals shall only be removed from Rev B and later versions.	4674
	In Section 5.1, ” Schematics”, 7/11 edited	5083
	n Section 5.1, ” Schematics”, Rev B changed into Rev A in 3/11	5625
	Row R30 and note (2) added to Table 4-1 on page 4-1	6056

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